Loss-Constrained Optimized Pulse Patterns for Three-Level Converters with Robustness to Power Factor Variations

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Abstract—This paper presents the computation of three-level optimized pulse patterns (OPPs) that limit the converter losses and are robust to power factor variations. By constraining the switching and conduction losses in the optimization process the trade-off between converter losses and current harmonic distortions can be improved. Moreover, to increase the solution space of the loss-constrained OPP problem, and thus have more degrees of freedom when establishing the Pareto optimal solutions, the symmetry properties of conventional OPPs are relaxed. Additionally, by constraining the losses not only for a specific power factor but for a range of them, the variation of the losses is small when varying the power factor. As a result, the converter efficiency is improved over a wide range of operating points, as shown with the presented results.

Index Terms—Modulation scheme, pulse width modulation (PWM), optimized pulse patterns (OPPs), medium-voltage converters, three-level converters

I. Introduction

Neutral-point-clamped (NPC) converters are typically used in medium-voltage (MV) drive systems. In such applications, the switching losses are high due to the high dc-link—and thus blocking—voltage and commutated currents. To keep the switching losses low, the switching frequency is usually kept below $250\,\text{Hz}$ [1]. This, however, increases the current harmonic distortions, which in turn lead to increased thermal losses in the machine. Therefore, the trade-off between the current harmonic distortions and converter losses is an important topic.

Conventional modulation techniques, such as carrier-based pulse width modulation (CB-PWM) and space vector modulation (SVM), can typically achieve low harmonic distortions for pulse numbers above 40. For low pulse numbers, however, the current ripple can be substantial. As a result, the performance of conventional modulation methods significantly deteriorates under such operating conditions [2]. Moreover, the switching losses with such methods are high since switching cannot be avoided when the commutated current is high.

To address the latter shortcoming of conventional modulation methods, and thus improve the efficiency of the converter, discontinuous PWM (DPWM) methods have been proposed [3]. With DPWM one of the three phases is clamped to the upper or lower rail of the dc link for one-third of the fundamental period, effectively reducing the switching frequency by 33.33%, and thus resulting in decreased switching losses [4]. To not compromise this feature, no additional switchings should occur when changing the clamping mode. For this reason, the voltage vectors need to be rearranged within the modulation cycle [5]. Additionally, DPWM can be modified to further minimize the switching losses. By properly adjusting the clamping intervals, commutations at high currents can be avoided, thus, further limiting the switching losses [6]. Moreover, the output quality of the current can be improved by also clamping the dc-link midpoint instead of only clamping the upper or lower dc-link rail [7]. Nevertheless, the quality of the output current remains worse than that of conventional modulation methods, while the implementation complexity is also higher.

An improved solution to reduce switching losses is programmed modulation techniques, such as selective harmonic elimination (SHE), or optimized pulse patterns (OPPs) [8]. By using OPPs, the switching frequency can be reduced by up to 25% compared with conventional PWM methods without sacrificing the harmonic performance [9]. This is due to the fact that OPPs are computed in an offline optimization procedure by minimizing the total demand distortion (TDD) of the stator current, while the switching frequency can be kept below a maximum switching frequency limit [10].

In [11], the current TDD for a given switching frequency is improved by relaxing the symmetry properties that are typically imposed on OPPs. In this work, it is shown that the trade-off between current TDD and power losses can be further improved by not only relaxing these properties but also constraining the losses. By adding a constraint to the optimization problem that accounts for the converter switching and conduction losses, an upper bound on them is guaranteed, ensuring safe operation and better utilization of the thermal capability of the semiconductor devices [12]. However, the total losses and therefore the resulting OPPs depend on the power factor, which is load- and operating-point dependent. To

avoid compromising the aforementioned trade-off—and thus the efficiency—the robustness of the computed OPPs under power factor changes must be considered. Hence, *robust* loss-constrained OPPs are proposed in this paper to ensure a high efficiency over a wider range of power factors. The presented numerical results verify this favorable behavior.

II. THREE-LEVEL OPPs WITH CONSTRAINED POWER LOSSES

Assuming a three-level converter, the switching signal $u(\theta) \in \{-1, 0, 1\}$ is a 2π-periodic signal with a fundamental frequency f_1. The pulse number is defined as the ratio $d = \frac{f_{sw}}{f_1}$, where f_{sw} is the average device switching frequency. The full-wave switching signal can be described by the $4d$ switching angles α_i, $i \in \{1, \ldots, 4d\}$, where a switching transition $\Delta u_i = u_i - u_{i-1} \in \{-1, 1\}$ occurs, with $u_i \in \{-1, 0, 1\}$, $i \in \{0, \ldots, 4d\}$, being the switch position. The switching angles of the OPPs are computed by minimizing an objective function that captures the load current TDD I_{TDD}. Note that the latter is proportional to the weighted sum of the switching harmonics $\hat{u}_n$ when an inductive load is assumed. For an analytical derivation of I_{TDD}, the reader is referred to [11].

Conventional OPPs assume three-phase and quarter- and half-wave symmetry (QaHWS), while all switch positions in the first half-period are non-negative, with the first switch position being zero, i.e., $u_0 = 0$. They can, therefore, be fully described using only the d switching angles $\boldsymbol{\alpha_Q} = [\alpha_1 \ \alpha_2 \ \ldots \ \alpha_d]^T \in [0, \pi/2]$.

The optimization problem to compute OPPs with QaHWS is

$$
\begin{aligned}
\underset{\boldsymbol{\alpha_Q}}{\text{minimize}} \quad & J(\boldsymbol{\alpha_Q}) = \sum_{n=5,7,\ldots} \left(\frac{b_n}{n}\right)^2 \\
\text{subject to} \quad & b_1 = m \\
& 0 \leq \alpha_1 \leq \alpha_2 \leq \ldots \leq \alpha_d \leq \frac{\pi}{2},
\end{aligned}
\tag{1}
$$

where $m \in [0, 4/\pi]$ is the desired modulation index, and b_n are the nonzero Fourier coefficients given by

$$
b_n = \frac{4}{n\pi} \sum_{i=1}^{d} \Delta u_i \cos(n\alpha_i).
$$

Note that even harmonics of QaHWS OPPs are zero, while triplen harmonics are not considered in the optimization problem as they do not drive harmonic currents in a three-phase load with a floating star point.

However, as shown in [11], the trade-off between harmonic distortions and losses can be improved by dropping the quarter-wave symmetry. By doing so, half-wave symmetric (HWS) OPPs result, meaning that $2d$ switching angles $\boldsymbol{\alpha_H} = [\alpha_1 \ \alpha_2 \ \ldots \ \alpha_{2d}]^T \in [0, \pi]$ are required instead.

Given the above, the optimization problem to compute OPPs with HWS is

$$
\begin{aligned}
\underset{\boldsymbol{\alpha_H}}{\text{minimize}} \quad & J(\boldsymbol{\alpha_H}) = \sum_{n=5,7,\ldots} \frac{a_n^2 + b_n^2}{n} \\
\text{subject to} \quad & a_1 = 0 \\
& b_1 = m \\
& 0 \leq \alpha_1 \leq \alpha_2 \leq \ldots \leq \alpha_{2d} \leq \pi,
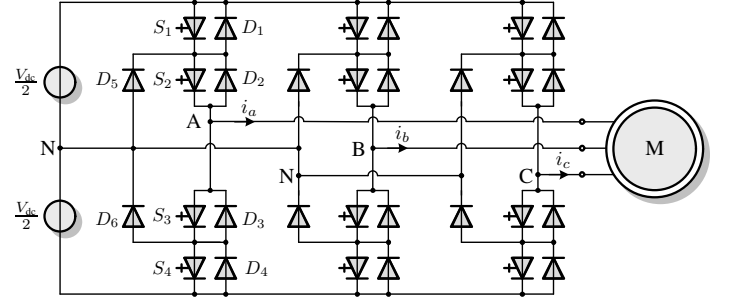\end{aligned}
\tag{2}
$$

Fig. 1: A three-level NPC converter driving a machine

TABLE I: Semiconductor parameters for loss calculations

GCT 5SHY 4045L0004	Diode D1961
$e_{on} = 1.029\,J$	
$e_{off} = 28.08\,J$	$e_{rr} = 15.2\,J$
$a_{GCT} = 0.97\,V$	$a_{diode} = 1.19\,V$
$b_{GCT} = 0.245 \cdot 10^{-3}\,V/A$	$b_{diode} = 0.395 \cdot 10^{-3}\,V/A$

where the nonzero a_n and b_n Fourier coefficients are

$$
a_n = -\frac{2}{n\pi} \sum_{i=1}^{2d} \Delta u_i \sin(n\alpha_i),
$$

$$
b_n = \frac{2}{n\pi} \sum_{i=1}^{2d} \Delta u_i \cos(n\alpha_i).
$$

Note that all even harmonics are zero with HWS as well.

A. Power Losses Calculation for an NPC Converter

A three-level NPC converter with a machine is shown in Fig. 1. In each phase, there are 4 active switches S_1 to S_4 with their respective freewheeling diodes D_1 to D_4, and two clamping diodes D_5 and D_6. In this work, the switching devices are the integrated-gate-commutated thyristor (IGCT) 5SHY 4045L0004 and the diode D1961. The parameters of the semiconductor devices at rated maximum values of $v_T = 2.4\,kV$ and $i_T = 4.5\,kA$ are given in Table I.

Usually, the losses of the converter are quantified by the switching frequency. However, the placement of the switching angles can significantly affect the losses as these heavily depend on the commutated current at the switching events and between them. For this reason, an analytical calculation of the losses is considered in this work, as shown in the sequel.

Since OPPs exhibit three-phase symmetry, it suffices to calculate the losses in one phase leg of the NPC converter. Additionally, to simplify the computation of the switching losses, the total dc-link voltage V_{dc} is assumed constant, and the fluctuations of the neutral point potential small. As a result, the blocking voltage of each semiconductor is half the dc-link voltage $v_T = \frac{V_{dc}}{2}$, and the losses depend only on the instantaneous value of the commutated current. The phase current $i_x(t)$ with $x \in \{a, b, c\}$, is considered sinusoidal with frequency f_1, i.e., $i_x(t) = \sin(2\pi f_1 t - \phi)$, where ϕ is the angular displacement between the phase current and voltage.

TABLE II: Switching energy losses in an NPC phase leg.

Polarity of phase current i_x	Switching transition	Switching energy losses
> 0	$0 \rightarrow 1$	$e_{\mathrm{on},S_1} + e_{\mathrm{rr},D_5}$
	$1 \rightarrow 0$	e_{off,S_1}
	$0 \rightarrow -1$	e_{off,S_2}
	$-1 \rightarrow 0$	$e_{\mathrm{on},S_2} + e_{\mathrm{rr},D_4}$
< 0	$0 \rightarrow 1$	e_{off,S_3}
	$1 \rightarrow 0$	$e_{\mathrm{on},S_3} + e_{\mathrm{rr},D_1}$
	$0 \rightarrow -1$	$e_{\mathrm{on},S_4} + e_{\mathrm{rr},D_6}$
	$-1 \rightarrow 0$	e_{off,S_4}

TABLE III: Conduction energy losses in an NPC phase leg.

Polarity of phase current i_x	Switch position	Conduction energy losses
> 0	1	$e_{\mathrm{con},S_1} + e_{\mathrm{con},S_2}$
	0	$e_{\mathrm{con},S_2} + e_{\mathrm{con},D_5}$
	-1	$e_{\mathrm{con},D_3} + e_{\mathrm{con},D_4}$
< 0	1	$e_{\mathrm{con},D_1} + e_{\mathrm{con},D_2}$
	0	$e_{\mathrm{con},S_3} + e_{\mathrm{con},D_6}$
	-1	$e_{\mathrm{con},S_3} + e_{\mathrm{con},S_4}$

The IGCTs produce switching (energy) losses e_{on} and e_{off} in turn-on and turn-off events, respectively. The switching losses of the IGCTs are assumed linear in the current, i.e.,

$$e_{\mathrm{on}} = c_{\mathrm{on}} \frac{V_{\mathrm{dc}}}{2} i_x \,, \tag{3a}$$

$$e_{\mathrm{off}} = c_{\mathrm{off}} \frac{V_{\mathrm{dc}}}{2} i_x \,, \tag{3b}$$

where the coefficients c_{on}, c_{off} are derived from the data sheets, and i_x is the instantaneous current at a switching event. On the contrary, the diodes have only turn-off losses—also called reverse-recovery losses e_{rr}—which are nonlinear in the current, i.e.,

$$e_{\mathrm{rr}} = c_{\mathrm{rr}} \frac{V_{\mathrm{dc}}}{2} f_{\mathrm{rr}}(i_x) \,, \tag{4}$$

where the function $f_{\mathrm{rr}}(i_x)$ and coefficient c_{rr} are derived from the data sheets.

The conduction (energy) losses e_{con} for both IGCTs and diodes are calculated based on the current. The on-state voltage drop is assumed affine in the current

$$v_T = a + b i_x \,, \tag{5}$$

where the parameters a_{GCT}, b_{GCT}, or a_{diode}, b_{diode}, are selected for a, b, depending on the conducting device. As a result, the conduction power losses are given by

$$p_{\mathrm{con}} = v_T(i_x) i_x = a i_x + b i_x^2 \,, \tag{6}$$

and the conduction energy is

$$e_{\mathrm{con}} = \int p_{\mathrm{con}} \,\mathrm{d}t = \int a i_x(t) + b i_x^2(t) \,\mathrm{d}t \,. \tag{7}$$

For the detailed computation of the losses, the reader is referred to [13, Section 2.3].

Depending on the polarity of the current and the switching transition, different devices turn on and off. The switching losses for a phase leg of an NPC converter are reported in Table II. Similarly, depending on the polarity of the current and the switch position, different devices conduct the current. The conduction losses for a phase leg of an NPC converter are reported in Table III.

In this work, both switching and conduction losses are taken into account. The total power losses are the average of the switching and conduction energy losses over the whole fundamental period $T_1 = 1/f_1$ in one phase of the NPC converter, i.e.,

$$P_{\mathrm{tot}} = \overbrace{\frac{\sum e_{\mathrm{on},S_1:S_4} + e_{\mathrm{off},S_1:S_4} + e_{\mathrm{rr},D_1:D_6}}{T_1}}^{P_{\mathrm{sw}}} + \underbrace{\frac{\sum e_{\mathrm{con},S_1:S_4} + e_{\mathrm{con},D_1:D_6}}{T_1}}_{P_{\mathrm{con}}} \,, \tag{8}$$

and can be calculated based on the applied OPP, phase current, and displacement angle ϕ. Hence, to find P_{tot}, the switching and conduction losses need to be calculated based on the semiconductor switches that commutate the current and the switching events, as described below.

At every switching angle α_i, the polarity of the current $i_x(\alpha_i)$ and the switch positions involved u_{i-1}, u_i, can be used to determine which devices turn on and off. For example, if $i_x(\alpha_i) > 0$ and $u_{i-1} = 0$, $u_i = 1$, it can be deduced from Table II that the top outer switch S_1 and the upper clamping diode D_5 produce turn-on and reverse-recovery losses, respectively, calculated based on (3a) and (4).

Assuming that the current does not change polarity between two consecutive switching angles, α_i, and α_{i+1}, the conduction losses in that interval are calculated by integrating (6) from α_i to α_{i+1}, where the coefficients a, b are selected with the help of Table III based on the polarity of $i_x(\alpha_i)$ and the switch position u_i. As a sinusoidal current is assumed for the loss calculations, it is implied that its polarity changes at $\phi + k\pi$, $k \in \mathbb{Z}$. Hence, if the subinterval formed by α_i and α_{i+1} does not include a current zero-crossing event, then the conducting devices do not change. As a result, the conduction losses in this subinterval are

$$e_{\mathrm{con}} = \frac{T_1}{2\pi} \int_{\alpha_i}^{\alpha_{i+1}} a i_x(\vartheta) + b i_x^2(\vartheta) \,\mathrm{d}\vartheta \,. \tag{9}$$

If, however, the current changes polarity in the subinterval $[\alpha_i, \alpha_{i+1}]$, i.e., $\alpha_i < \phi < \alpha_{i+1}$, the corresponding conduction losses are computed with the help of two subintegrals, i.e.,

$$e_{\mathrm{con}} = \frac{T_1}{2\pi} \int_{\alpha_i}^{\phi} a_{\mathrm{I}} i_x(\vartheta) + b_{\mathrm{I}} i_x^2(\vartheta) \,\mathrm{d}\vartheta + \frac{T_1}{2\pi} \int_{\phi}^{\alpha_{i+1}} a_{\mathrm{II}} i_x(\vartheta) + b_{\mathrm{II}} i_x^2(\vartheta) \,\mathrm{d}\vartheta \,, \tag{10}$$

where the coefficients a_{I}, b_{I}, and a_{II}, b_{II} are chosen depending on the conducting devices (see Table III).

(a) OPP with $P_{\text{tot}} = 10.6\,\text{kW}$ and $I_{\text{TDD}} = 13.21\%$

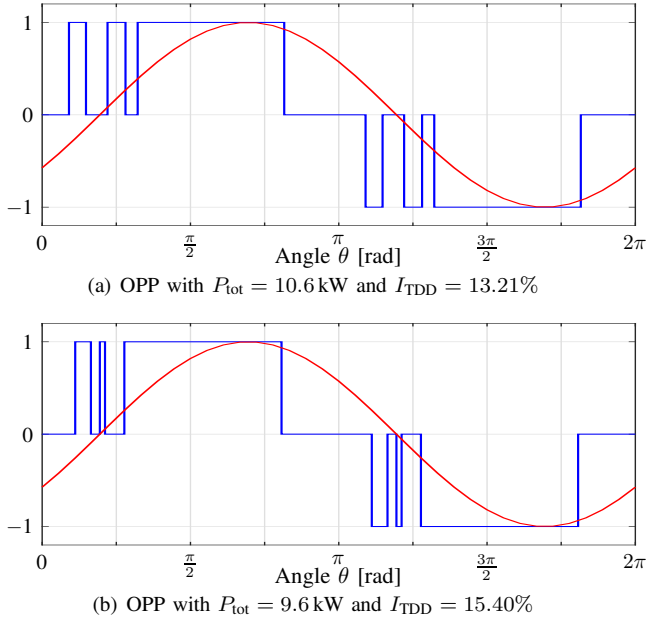(b) OPP with $P_{\text{tot}} = 9.6\,\text{kW}$ and $I_{\text{TDD}} = 15.40\%$

Fig. 2: HWS OPPs (blue) with different constraints on the losses for $d = 3$ at $m = 1$ and $\phi = 35°$. The phase current (red) is also shown.

B. Relaxed OPP Problem with Limited Power Losses

As shown in [14], OPPs can gain additional features by introducing suitable constraints to the OPP optimization problem. Motivated by this, the constraint

$$P_{\text{tot}}(\boldsymbol{\alpha}, \phi) \leq P_{\text{lmt}}, \tag{11}$$

is added to the optimization problem (1) or (2) such that loss-constrained OPPs can be computed. In (11), P_{lmt} is the chosen limit on the total power losses and $\boldsymbol{\alpha}$ is either $\boldsymbol{\alpha}_Q$ or $\boldsymbol{\alpha}_H$ depending on whether QaHWS or HWS, respectively, is required. Note that, as also shown in Section III, different OPPs result by adjusting P_{lmt}, see, e.g., the illustrative example in Fig. 2 for $\phi = 35°$ and $m = 1$. Specifically, the HWS patterns in Figs. 2(a) and 2(b) result for the limits $P_{\text{lmt}} = 10.6\,\text{kW}$ and $P_{\text{lmt}} = 9.6\,\text{kW}$, respectively. As can be observed, as the upper limit on the permissible total semiconductor losses in one phase gets tighter, the switching angles are moved closer to the zero crossing of the current. However, this comes at a cost of increased current distortions. In the considered example, the current TDD increases by 16.6% when the losses are decreased by $1\,\text{kW}$ per phase, i.e., for a 9% relative decrease in the power losses.

1) Pulse Dropping: According to the optimization problems (1) and (2), two consecutive switching angles have to meet constraints of the form

$$\alpha_i \leq \alpha_{i+1}. \tag{12}$$

In the corner case $\alpha_i = \alpha_{i+1}$, the two switching transitions cancel each other out, and no switching occurs at α_i. This case is referred to as *pulse dropping*. This feature enables the computation of OPPs with $\leq 2d$ switching angles in one half-period when solving the optimization problem for pulse number d. This means that if a pattern with $d - 1$ pulses can

meet the power loss constraint while achieving lower current TDD than any pattern with d pulses, the unnecessary pulses are dropped, and it is returned as the optimal solution, without having to solve the optimization problem for $d - 1$.

However, even though constraint (12) allows for overlapping switching angles to be removed, it does not prevent the existence of pulses of infinitesimal width, i.e., in the range of a few μs. The voltage-second contribution of such pulses as well as their effect on the current TDD are insignificant. On the other hand, their presence can give rise to significant switching losses. Moreover, such short pulses are not allowed in a physical system as a minimum on/off time Δt_{min} is required by the devices.

To account for the above, (12) can be modified such that pulses shorter than Δt_{min} are prevented. To this aim, two consecutive switching angles need to have a minimum difference, as dictated by the minimum on/off time Δt_{min}. Hence, the following constraint on the switching angles can be considered

$$\alpha_i + 2\pi \frac{\Delta t_{\text{min}}}{T_1} \leq \alpha_{i+1}, \tag{13}$$

where Δt_{min} is set to $50\,\mu$s to define the minimum pulse width.

However, the (desirable) pulse-dropping feature is removed with constraint (13). To overcome this issue, an approach that combines constraint (12) with the minimum pulse width requirement is eventually adopted. More specifically, pulses smaller than Δt_{min} are not considered in the losses calculation process, while the corresponding switching angles that generate such pulses are set equal in the optimization process, i.e., $\alpha_i = \alpha_{i+1}$. This way, pulses are allowed to drop, as the pulse-dropping feature is active, while no pattern with pulses shorter than Δt_{min} can be considered optimal.

C. Robust Loss-Constrained OPPs

Since the instantaneous current depends on the displacement angle ϕ, the total losses vary with ϕ. This implies that the loss-constrained OPP problem needs to be solved for multiple displacement angles ϕ. This, however, significantly increases the computational and memory requirements. As an example, consider the HWS OPP shown in Fig. 3. This pattern is computed to achieve total power losses of $P_{\text{tot}} = 10.2\,\text{kW}$ when a displacement angle of $\phi = 35°$ is considered, see Fig. 3(a). However, as shown in Fig. 3(b), if the displacement angle changes to $\phi = 45°$, the same OPP will result in $P_{\text{tot}} = 10.66\,\text{kW}$. This increase in P_{tot} is due to the narrow pulse occurring at the current zero crossing (at $\theta \approx 35°$) in Fig. 3(a); when the displacement angle changes to $\phi = 45°$ the switching events happen at a nonzero current, thus generating switching losses. As a result, the losses are redistributed among the semiconductor devices, see Fig. 3(c). As can be seen, the switching losses are moved from the outer switches S_1, S_4, and clamping diodes D_5, D_6, to the inner switches S_2, S_3, and outer diodes D_1, D_4, and the total losses are increased.
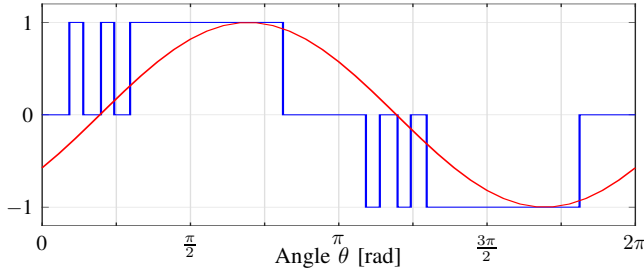
(a) At displacement angle $\phi = 35°$ the total losses are $P_{tot} = 10.20\,\text{kW}$
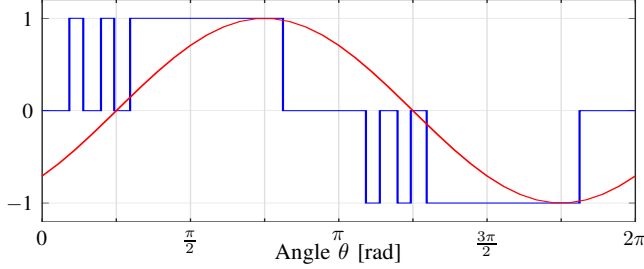
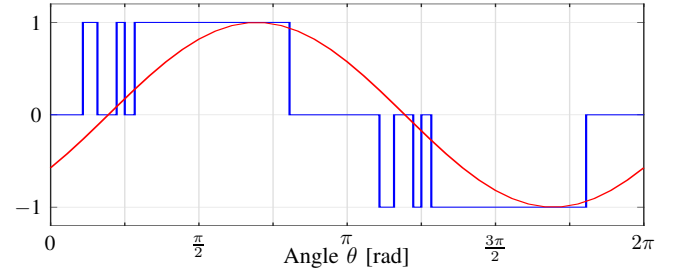

(b) At displacement angle $\phi = 45°$ the total losses are $P_{tot} = 10.66\,\text{kW}$
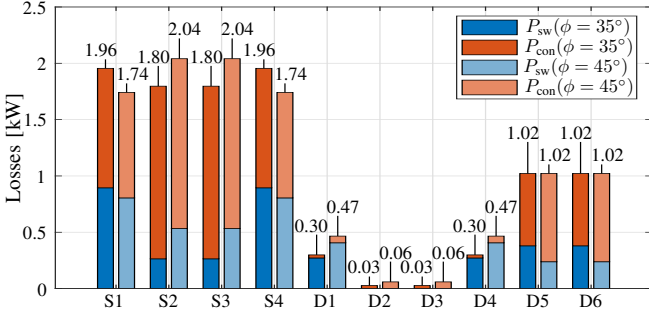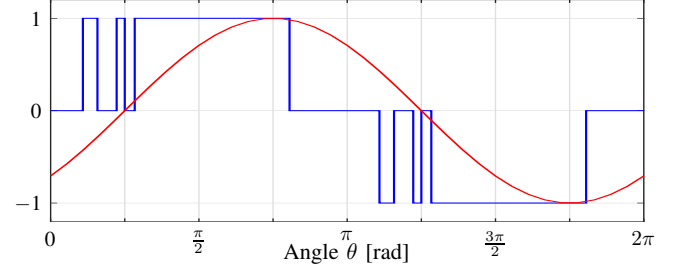

(c) Losses distribution. The switching and conduction losses at $\phi = 35°$ are shown with blue and orange, respectively. The switching and conduction losses at $\phi = 45°$ are shown with light blue and light orange, respectively.
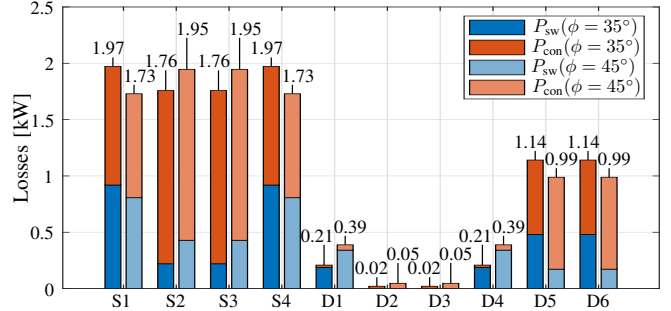
Fig. 3: HWS OPP (blue) with $d = 3$ and $m = 1$, and phase current (red) at different displacement angles. The current TDD is $I_{TDD} = 13.73\%$.

(a) At displacement angle $\phi = 35°$ the total losses are $P_{tot} = 10.20\,\text{kW}$

(b) At displacement angle $\phi = 45°$ the total losses are $P_{tot} = 10.20\,\text{kW}$

(c) Losses distribution. The switching and conduction losses at $\phi = 35°$ are shown with blue and orange, respectively. The switching and conduction losses at $\phi = 45°$ are shown with light blue and light orange, respectively.

Fig. 4: *Robust* HWS OPP (blue) with $d = 3$ and $m = 1$, and phase current (red) at different displacement angles. The current TDD is $I_{TDD} = 14.67\%$.

Given this, and considering that the power factor changes during operation, OPPs that can achieve near-optimal performance for a range of operating points would be advantageous. To minimize the variation of the losses when the OPPs are used with different displacement angles they were optimized for, a modification in constraint (11) is proposed. More specifically, the total losses with $\phi \pm \Delta\phi$, where $\Delta\phi$ is a variation in ϕ, are also constrained, thus resulting in the constraint

$$P_{tot}(\boldsymbol{\alpha}, \phi - \Delta\phi) \leq P_{lmt} \text{ and}$$
$$P_{tot}(\boldsymbol{\alpha}, \phi) \leq P_{lmt} \text{ and} \quad (14)$$
$$P_{tot}(\boldsymbol{\alpha}, \phi + \Delta\phi) \leq P_{lmt}.$$

Notice that to ensure robustness, the OPP problem (1) or (2) is solved with constraint (14) instead of (11). In doing so, the OPPs are not optimized with respect to one power factor (i.e., displacement angle) but over a range of displacement angles. This increases the robustness of the loss-constrained OPPs, thus ensuring maximization of the drive efficiency for a given I_{TDD} over a range of power factors.

To illustrate the robustness of these OPPs, a *robust* HWS pattern with $\phi = 35°$ and $\Delta\phi = 10°$ is considered in Fig. 4.

This OPP achieves similar losses to the pattern in Fig. 3 when $\phi = 35°$. Notice that compared to the pattern in Fig. 3 the short pulse close to the zero crossing of the current is narrower and occurs at a bigger angle. As a result, the increase in the losses is smaller when the pattern is used with displacement angle $\phi = 45°$ ($\Delta\phi = 10°$). It should be noted that the robustness feature comes at the expense of a slight increase in the current TDD; I_{TDD} increases from 13.73% to 14.67% in the discussed example, i.e., a 6.8% relative increase is observed. Finally, increasing the robustness of OPPs to power factor variations also affects the distribution of the losses among the semiconductor devices, as visualized in Fig. 4(c). When the pattern optimized for $\phi = 35°$—while accounting for a variation of $\Delta\phi = 10°$—is used at displacement angle $\phi = 45°$, the switching losses are moved from the outer switches S_1, S_4 and clamping diodes D_5, D_6 to the inner switches S_2, S_3 and outer diodes D_1, D_4, and the total losses are increased. This increase, however, is smaller than in Fig. 3 because the commutations near the zero crossing of the current occur at lower currents.
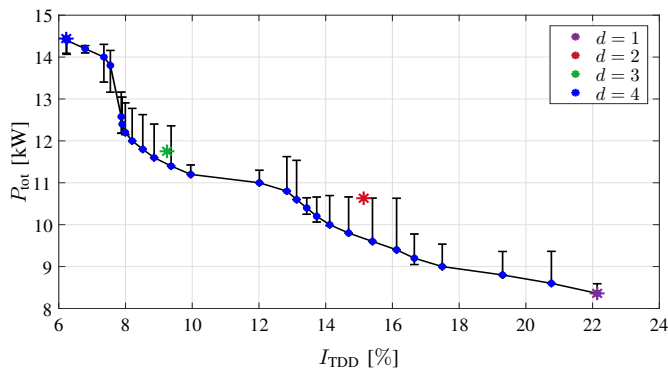
(a) Loss-constrained HWS OPPs for $d = 4$
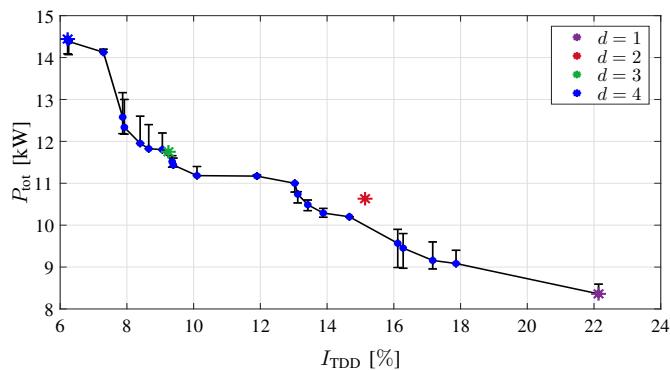
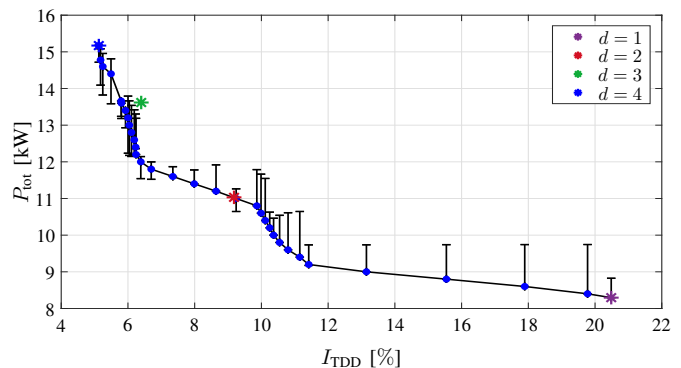(b) *Robust* loss-constrained HWS OPPs for $d = 4$

Fig. 5: Total power losses versus current TDD at $m = 1$, $\phi = 35°$, and up to $d = 4$. Conventional QaHWS OPPs are shown with asterisks, and loss-constrained HWS OPPs are depicted with solid (blue) circles. The variation of the power losses with a changing power factor is also shown considering a variation $\Delta\phi = \pm10°$.

(a) Loss-constrained HWS OPPs for $d = 4$

(b) *Robust* loss-constrained HWS OPPs for $d = 4$

Fig. 6: Total power losses versus current TDD at $m = 1.1$, $\phi = 35°$, and up to $d = 4$. Conventional QaHWS OPPs are shown with asterisks, and loss-constrained HWS OPPs are depicted with solid (blue) circles. The variation of the power losses with a changing power factor is also shown considering a variation $\Delta\phi = \pm10°$.
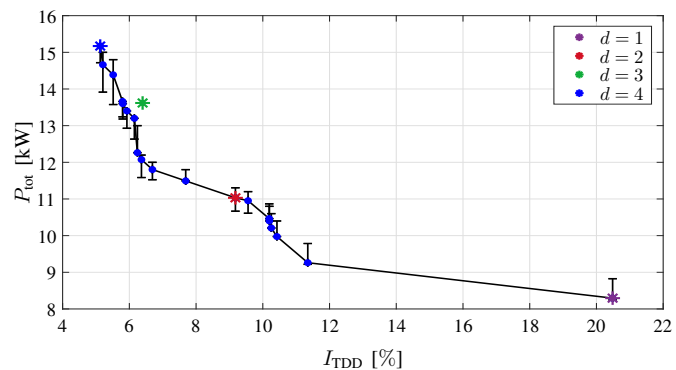
III. NUMERICAL RESULTS

The performance and features of the OPPs in question are discussed hereafter. All OPPs are computed for an MV drive system consisting of a squirrel cage induction machine with $3.55\,\mathrm{kV}$ rated voltage, $2.2\,\mathrm{kA}$ rated current, $50\,\mathrm{Hz}$ nominal frequency, 0.23 per unit (p.u.) total leakage reactance, and a three-level inverter with a dc-link voltage of $V_{\mathrm{dc}} = 4.8\,\mathrm{kV}$.

A. Pareto Fronts for Displacement Angle $\phi = 35°$

This section compares the unconstrained QaHWS OPPs to HWS OPPs (problem (2)) with (a) the loss constraint (11) (see Figs. 5(a), 6(a), and 7(a)) and (b) constraint (14) (see Figs. 5(b), 6(b), and 7(b)) in terms of total power losses and I_{TDD}. For demonstration purposes, the OPPs are calculated at modulation indices $m = 1$, $m = 1.1$, and $m = 1.2$, and $\phi = 35°$, see Figs. 5, 6, and 7, respectively. The unconstrained QaHWS OPPs are shown as asterisks with a color indicating the pulse number, i.e., $d = 1$ is purple, $d = 2$ red, $d = 3$ green, and $d = 4$ blue. For the loss-constrained OPPs shown in the same figures only $d = 4$ is considered, while P_{lmt} is changed from 16 to $8\,\mathrm{kW}$ with a step of $0.2\,\mathrm{kW}$. The individual loss-constrained OPPs are shown as solid blue circles, while the corresponding Pareto front is shown with a black solid line. The error bars indicate the total loss variation when $\Delta\phi = \pm10°$ is considered.

For example, considering $m = 1$, as seen in Fig. 5(a), by relaxing the QaHWS to HWS, the Pareto front moves towards the origin. With respect to the unconstrained QaHWS OPP for $d = 2$, a reduction in the total losses up to $1\,\mathrm{kW}$ per phase, i.e., 9% relative improvement, can be achieved without compromising the current TDD, resulting in improved efficiency, and thus significant energy savings. Equivalently, compared with the unconstrained QaHWS OPP for $d = 2$, the I_{TDD} of the loss-constrained HWS OPPs can be reduced by up to 13% without increasing the losses, resulting in an improved overall performance and less thermal losses in the motor. A similar behavior is observed for $m = 1.1$, as can be seen in Fig. 6(a). The loss-constrained HWS OPPs can reduce the total losses by $1.6\,\mathrm{kW}$ per phase compared to the unconstrained QaHWS OPP for $d = 3$, i.e., 12% relative improvement, while producing the same current TDD. Correspondingly, the loss-constrained HWS OPPs can result in similar losses to the unconstrained QaHWS OPP for $d = 3$ while reducing the I_{TDD} by up to 9.3%. However, as the modulation index increases, e.g., for $m = 1.2$, the conventional OPPs become embedded in the Pareto front of the loss-constrained HWS OPPs due to the limited degrees of freedom, see Fig. 7(a).

Nevertheless, the losses of the HWS loss-constrained OPPs vary with the change of the displacement angle ϕ. For example, the OPPs in Fig. 5(a) result in higher losses when ϕ changes by $\Delta\phi = \pm10°$, e.g., the OPP with $I_{\mathrm{TDD}} = 13.7\%$ has

(a) Loss-constrained HWS OPPs for $d = 4$
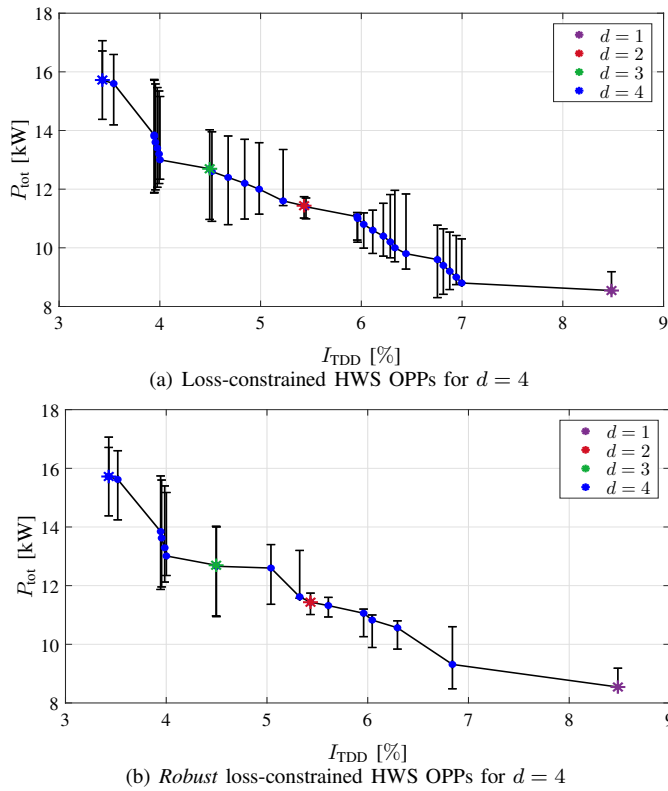

(b) *Robust* loss-constrained HWS OPPs for $d = 4$

Fig. 7: Total power losses versus current TDD at $m = 1.2$, $\phi = 35°$, and up to $d = 4$. Conventional QaHWS OPPs are shown with asterisks, and loss-constrained HWS OPPs are depicted with solid (blue) circles. The variation of the power losses with a changing power factor is also shown considering a variation $\Delta\phi = \pm 10°$.

$P_{\text{tot}}(\phi = 35°) = 10.2 \text{ kW}$ while $P_{\text{tot}}(\phi = 45°) = 10.66 \text{ kW}$, see Fig. 3. As shown in Fig. 5(b), however, this issue is successfully addressed with the robust OPPs. Specifically, when the robust OPPs optimized for $\phi = 35°$ are used for, e.g., $\phi = 45°$, the losses do not increase much, see also the example in Fig. 4, thus, the efficiency remains high even when the power factor changes. This point is highlighted, when comparing Figs. 5(a) and 5(b). As can be seen, the OPPs in Fig. 5(b) exhibit a smaller loss variation, while the overall performance (i.e., the trade-off between total power losses P_{tot} and current distortions I_{TDD}) remains significantly better compared with that of conventional, i.e., unconstrained QaHWS, OPPs. Hence, the proposed OPPs not only improve the converter efficiency for a given I_{TDD} but are also robust to variations in the power factor. In doing so, the operation of the drive with as low converter power losses as possible is ensured over a wide range of operating points. Similar behavior is exhibited for all three modulations, see Figs. 5 to 7.

B. Pulse Dropping

For the loss-constrained HWS OPPs shown in this work, the optimization problem is solved only for $d = 4$, while P_{lmt} is changed from 16 to 8 kW with a step of 0.2 kW. However, as the constraint gets tighter, to achieve very low losses, pulses need to be dropped. More specifically, the conventional OPP for $m = 1$ has $I_{\text{TDD}} = 6.22\%$ and results in total losses
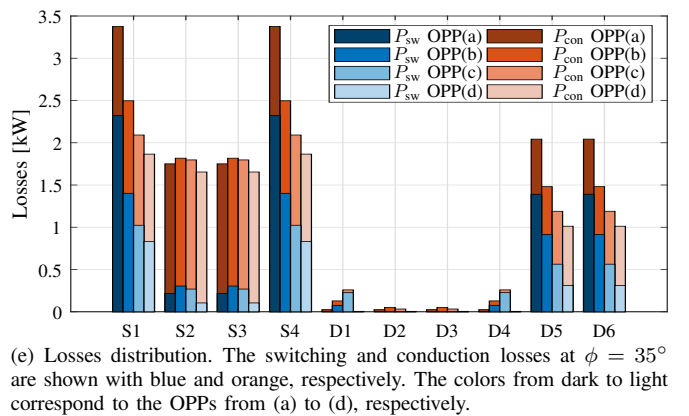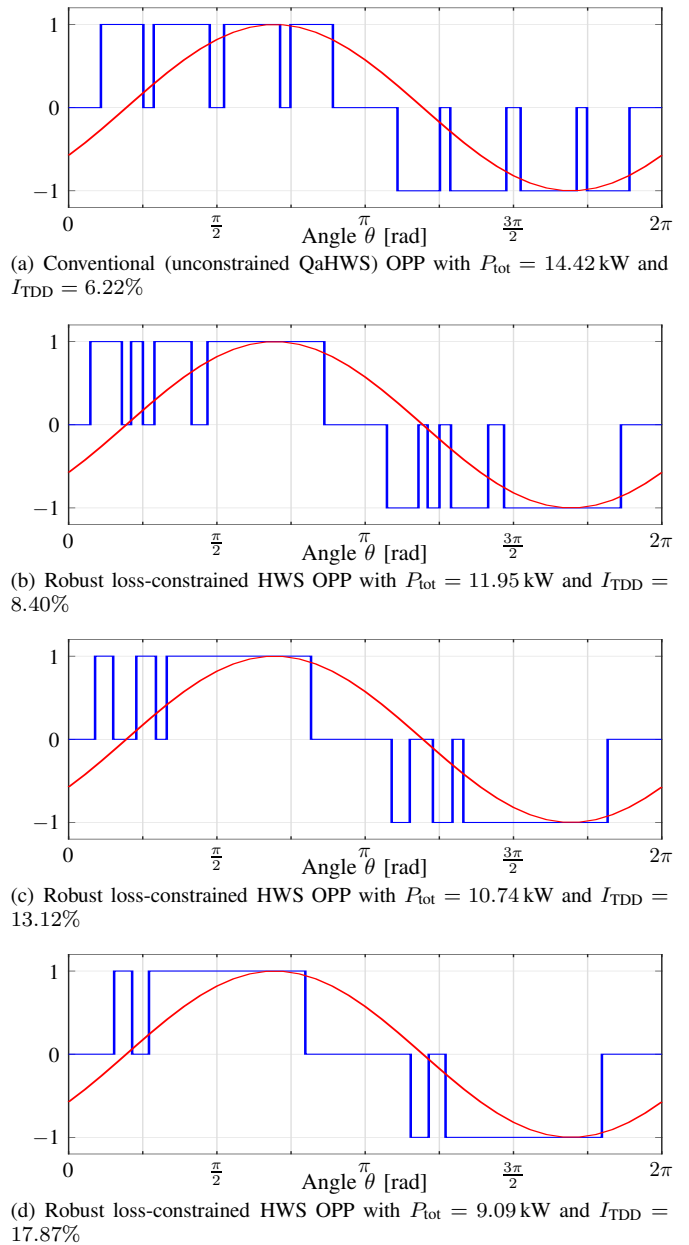

(a) Conventional (unconstrained QaHWS) OPP with $P_{\text{tot}} = 14.42 \text{ kW}$ and $I_{\text{TDD}} = 6.22\%$

(b) Robust loss-constrained HWS OPP with $P_{\text{tot}} = 11.95 \text{ kW}$ and $I_{\text{TDD}} = 8.40\%$

(c) Robust loss-constrained HWS OPP with $P_{\text{tot}} = 10.74 \text{ kW}$ and $I_{\text{TDD}} = 13.12\%$

(d) Robust loss-constrained HWS OPP with $P_{\text{tot}} = 9.09 \text{ kW}$ and $I_{\text{TDD}} = 17.87\%$

(e) Losses distribution. The switching and conduction losses at $\phi = 35°$ are shown with blue and orange, respectively. The colors from dark to light correspond to the OPPs from (a) to (d), respectively.

Fig. 8: OPPs with different constraints on the losses for $d = 4$, $m = 1$, and $\phi = 35°$ along with the phase current (red).

$P_{\text{tot}} = 14.42\,\text{kW}$ for $\phi = 35°$, see Fig. 8(a). When reducing the limit on the total losses, the pulses are rearranged within the period so that the switching actions occur at low current, see Fig. 8(b). This way, the total losses can be reduced by $2.47\,\text{kW}$ per phase, i.e., a 17.1% relative decrease is achieved, but at the cost of increased current distortions, with a relative increase of 35% in I_{TDD}.

The switching and conduction losses of the different patterns at $\phi = 35°$ presented in Fig. 8 are shown in Fig. 8(e) with blue and orange, respectively. As can be seen, when moving from the pattern of Fig. 8(a) to that of Fig. 8(b), the switching losses of the outer switches S_1, S_4 and clamping diodes D_5, D_6 get significantly lower. As the upper bound on the permissible losses is further reduced, the pulses get narrower and, eventually, pulses are dropped such that the switching losses can be reduced. In the case of $P_{\text{tot}} = 10.74\,\text{kW}$, see Fig. 8(c), the OPP has three pulses, and the total losses are reduced by $3.68\,\text{kW}$ per phase, i.e., 25.5% relative reduction compared to the unconstrained QaHWS OPP. However, the I_{TDD} is roughly twice that of the conventional OPP with four pulses. If the limit in the total losses is further decreased, additional pulses are dropped. To achieve total losses $P_{\text{tot}} = 9.09\,\text{kW}$, two pulses are dropped, resulting in the pulse number $d = 2$. In that case, the total losses are merely 63% of the total losses of the conventional OPP, but the harmonic distortions in the output current are nearly three times higher. From these results, the trade-off between the total losses and the harmonic distortions in the output current is clear.

At this point, it is worth discussing the effectiveness of the pulse-dropping feature of this optimization problem. All OPPs discussed in this section are produced by solving the optimization problem for $d = 4$. This provides some more degrees of freedom when more losses are tolerated. However, as the upper limit becomes tighter, pulses begin to drop, implying that the same results can be achieved when OPPs with a smaller pulse number (e.g., $d = 3$) are computed in the first place. This behavior implies that it suffices to solve the loss-constrained OPP problem with as high a pulse number as possible, since, depending on the value of the power loss constraint, OPPs with all possible pulse numbers result.

Finally, from Fig. 8(e), it is apparent that the conduction losses are almost the same regardless of the limit on the total losses. To achieve a specific modulation index a certain voltage-second contribution is required. Even when the pulses are rearranged and the conducting devices change from GCTs to diodes, the conduction losses are not that different due to the similar parameters of the two types of devices. This highlights that for the used devices, the switching losses are those that affect the converter efficiency. Therefore, to reduce the losses, first, the pulses are moved closer to the zero crossing of the current. Following, as the limit on the losses gets tighter, pulses are dropped to further decrease the switching losses.

IV. Conclusion

This paper proposed the computation of OPPs with limited total losses and robustness to power factor variations. The relaxation of the OPP symmetry properties allows rearranging the switching angles within the fundamental period to achieve switching at low currents, and hence reduce the switching losses. Additionally, by considering the variation of the power factor in the optimization problem, the total losses do not vary significantly with the variation of the displacement angle. As a result, low losses are guaranteed for a wide range of operating points. As demonstrated by the presented numerical results, the proposed OPPs significantly improve the fundamental trade-off between current distortions and power losses, while ensuring the highest possible converter efficiency over a wide range of operating points.

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