# Loss-Constrained Three-Level Optimized Pulse Patterns with Robustness to Power Factor Variations

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***Abstract*—This paper presents the computation of three-level optimized pulse patterns (OPPs) that limit the converter losses while maintaining robustness against power factor variations. By constraining the switching and conduction losses of each semiconductor switch in the optimization process the trade-off between semiconductor losses and current harmonic distortions is improved. Moreover, to expand the solution space of the loss-constrained optimization problem, and thus increase the degrees of freedom in the optimization process, the symmetry properties of conventional OPPs are relaxed. Furthermore, to enhance the robustness of the proposed OPPs to changes in the power factor, the optimization problem constrains the semiconductor losses over a range of power factors rather than a single one, thereby reducing loss variation under different load conditions. As a result, the worst-case losses, and therefore the worst-case junction temperature, are reduced over a wide range of operating points, as shown with the presented numerical results.**

***Index Terms*—Optimized pulse patterns (OPPs), three-level converters, synchronous optimal pulse width modulation (PWM), semiconductor losses, medium-voltage (MV) drives.**

## I. Introduction

THE three-level neutral-point-clamped (NPC) converter is commonly used in medium-voltage (MV) drive systems due to its performance advantages [1]. However, a key challenge with NPC converters is the unequal distribution of losses among the semiconductor switches [2], leading to uneven thermal stress. Since the thermal stress is a major factor in switch failures [3], it is important to keep it at bay. The thermal stress is closely linked to the switching losses, which are dominant in MV applications because of the high dc-link voltage and commutated currents. Therefore, to meet the thermal requirements, the switching losses are typically indirectly minimized by keeping the switching frequency bounded, usually below a few hundred hertz [4].

The performance of conventional modulation techniques, such as carrier-based pulse width modulation (CB-PWM) and space vector modulation (SVM), significantly deteriorates at low fundamental-to-switching frequency rations, i.e., pulse numbers [5]. To partially mitigate this issue, synchronized SVM can be employed. A carrier-based implementation of synchronized PWM is also possible [6]. Nevertheless, these methods still produce high switching losses because switching oftentimes occurs when the commutated current is high. To address this, discontinuous PWM (DPWM) methods have been proposed [7]. Specifically, DPWM reduces the switching losses by clamping one of the three phases to the upper or lower rail of the dc link for one-third of the fundamental period, effectively reducing the switching frequency by $33.33\%$ [8].

To maintain this feature, no additional switchings should occur when transitioning between clamping modes. For this reason, the voltage vectors need to be rearranged within the modulation cycle [9]. Nevertheless, the converter losses depend not only on the switching frequency but also on the employed modulation strategy [10]. Therefore, DPWM can be modified to further reduce the switching losses. By properly adjusting the clamping intervals, switching events can be avoided when the commutated current is high [11], [12]. Moreover, the output quality of the current can be improved by clamping not only the upper or lower dc-link rail but also to the dc-link midpoint [13]. Nonetheless, the trade-off between reduced power losses and harmonic distortions should be considered. In this regard, [14] proposed employing DPWM selectively, activating it only after the devices reach a critical remaining lifetime threshold. Another alternative is hybrid modulation that combines continuous and discontinuous modulation [15].

The above-mentioned methods can effectively reduce the total power losses, but they fail to adequately address the issue of uneven loss distribution. To relieve the most stressed device, the modulation techniques need to be adjusted. In this direction, [16] and [17] proposed leveraging the redundant voltage vectors of the NPC converter to relieve the most thermally stressed devices. In a similar fashion, [18] and [19] demonstrated that careful selection of the NPC converter voltage vectors leads to a more balanced loss distribution among the semiconductor switches. Moreover, [20] showed that using two-level SVM at low modulation indices can also improve the loss distribution. However, these methods are suitable for low or medium modulation indices, thus they cannot fully utilize the available dc-link voltage. To achieve operation across a wider range of modulation indices, conventional PWM methods need to be modified. For example, [21] achieved favorable loss management by combining unipolar and bipolar switch positions, albeit at the expense of worsened current harmonic performance. An alternative is to redistribute the losses by means of zero-sequence voltage (ZSV) injection, as proposed in [22]. The efficacy of this approach, however, depends on the power factor, with better loss redistribution occurring at power

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factors near zero, and diminishing effectiveness as the power factor approaches $\pm 1$. Additionally, by properly adjusting the ZSV injection the losses can be redistributed among the three phases [23]. Nevertheless, the extent of loss reduction on the most stressed device depends on the amount of ZSV injection; higher injection leads to greater loss reduction, but at the cost of higher current harmonic distortions. Hence, a trade-off emerges between minimizing losses on the most stressed device and maintaining acceptable current harmonics.

An improved solution to reduce switching losses, particularly at low pulse numbers, is programmed modulation techniques, such as selective harmonic elimination (SHE) or optimized pulse patterns (OPPs) [24]. By using OPPs, the switching frequency can be reduced by up to $25\%$ compared to conventional PWM methods without sacrificing the harmonic performance [25]. Alternatively, when compared to conventional PWM methods operating at the same switching frequency, OPPs simultaneously reduce harmonic distortions and motor losses [26]. This advantage arises because OPPs are computed through an offline optimization process, where the total demand distortion (TDD) of the stator current is minimized while ensuring the switching frequency remains below a predefined maximum [27]. Moreover, the harmonic performance of OPPs can be further enhanced by improving the accuracy of the system model. For instance, OPPs that account for the magnetic anisotropy of permanent magnet synchronous motors (PMSMs) were proposed in [28]–[31]. Additionally, [32] demonstrated that relaxing the symmetry properties topically imposed on OPPs can lead to additional improvements in current TDD for a given switching frequency.

The trade-off between current TDD and power losses of each semiconductor device can be further improved by not only relaxing the symmetry properties but also by constraining the total losses of each device. In this context, [33] introduced a modified OPP problem that bounds the total losses of each device while still producing currents of high quality. By doing so, the safe operation of the switches can be guaranteed. However, the total semiconductor losses–and consequently the resulting OPPs—depend on the power factor, which varies with the load and operating point. To ensure optimal performance across a range of power factors, the optimization problem must be solved for multiple operating points, necessitating a fine-gridding of the angular displacement between the phase current and voltage. This approach, however, significantly increases the number of lookup tables (LUTs) required to store the optimal switching angles. To reduce memory demands, only a limited number of power factors are typically considered, which leads to variations in semiconductor losses as the power factor changes. To avoid compromising the aforementioned trade-off, it is essential to account for the robustness of the computed OPPs under power factor variations, as discussed in [34]. In doing so, the losses can be maintained below the desired threshold across a range of operating points, achieving a balance between memory efficiency and optimal performance characterized by reduced current harmonic distortions and converter power losses.

This paper builds upon the work presented in [34] by extending the robustness concept to an optimization problem that considers the power losses of each semiconductor switch individually, rather than focusing solely on the total losses across all devices. Moreover, the proposed OPPs are optimized not just for a single operating point but for a range of conditions, enabling better utilization of the thermal capacity of the switches over a wider range of power factors. The presented results demonstrate that the proposed method allows for more effective loss distribution across varying power factors, leading to enhanced converter-friendly operation. Finally, to illustrate the practical value from an industrial perspective, numerical results are provided that show how the proposed method can increase the rated power of the semiconductor devices without exacerbating the thermal stress on them.

This paper is structured as follows. Section II outlines the computation of the semiconductor losses along with the strategy adopted to limit them. Additionally, the formulation of the relevant OPP optimization problem is presented. Sections III and IV provide numerical results for a specific operating point as well as a broader range of operating points, respectively. Finally, Section V concludes this paper.

## II. Three-Level OPPs with Constrained Power Losses

Assuming a three-level converter, the switching signal $u(\theta) \in \{-1, 0, 1\}$ is a $2\pi$-periodic signal with a fundamental frequency $f_1$. The pulse number is defined as the ratio $d = \frac{f_{\text{sw}}}{f_1}$, where $f_{\text{sw}}$ is the average device switching frequency. The full-wave switching signal can be described by the $4d$ switching angles $\alpha_i$, $i \in \{1, \ldots, 4d\}$, where a switching transition $\Delta u_i = u_i - u_{i-1} \in \{-1, 1\}$ occurs, with $u_j \in \{-1, 0, 1\}$, $j \in \{0, \ldots, 4d\}$, being the switch position. The switching angles of the OPPs are computed by minimizing an objective function that captures the load current TDD $I_{\text{TDD}}$. Note that the latter is proportional to the weighted sum of the switching harmonics $\hat{u}_n$ when an inductive load is assumed. For an analytical derivation of $I_{\text{TDD}}$, the reader is referred to [32].

Conventional OPPs assume three-phase and quarter- and half-wave symmetry (QaHWS). In this setup, all switch positions in the first half-period are non-negative, with the first switch position being zero, i.e., $u_0 = 0$. Consequently, conventional OPPs can be fully described using only the $d$ switching angles $\boldsymbol{\alpha}_Q = [\alpha_1 \ \alpha_2 \ \ldots \ \alpha_d]^T \in [0, \pi/2]^d$, while the pulse pattern structure, defined by the switch positions, is deterministic.

The optimization problem to compute OPPs with QaHWS is

$$\begin{aligned} \underset{\boldsymbol{\alpha_Q}}{\text{minimize}} \quad & J(\boldsymbol{\alpha_Q}) = \textstyle\sum_{n=5,7,\ldots} \left(\frac{b_n}{n}\right)^2 \\ \text{subject to} \quad & b_1 = m \\ & 0 \le \alpha_1 \le \alpha_2 \le \ldots \le \alpha_d \le \tfrac{\pi}{2}\,, \end{aligned} \tag{1}$$

where $m \in [0, 4/\pi]$ is the desired modulation index, and $b_n$ are the nonzero Fourier coefficients of the periodic pulse pattern given by

$$b_n = \frac{4}{n\pi} \sum_{i=1}^{d} \Delta u_i \cos(n\alpha_i)\,.$$

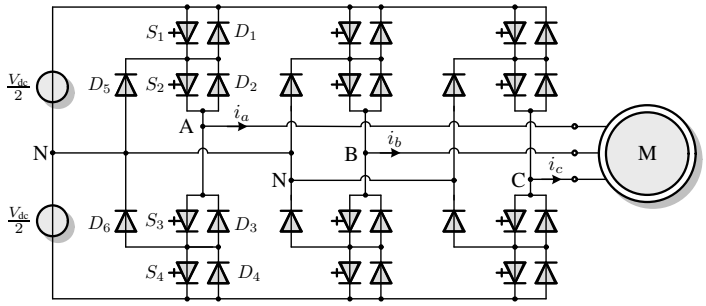



Fig. 1: A three-level NPC converter driving a machine.

TABLE I: Semiconductor device parameters

| | | |
|---|---|---|
| GCT 5SHY 4045L0004 | | |
| Turn-on losses | $e_{\text{on}}$ | $1.029\,\text{J}$ |
| Turn-off losses | $e_{\text{off}}$ | $28.08\,\text{J}$ |
| GCT coefficient | $a_{\text{GCT}}$ | $0.97\,\text{V}$ |
| GCT coefficient | $b_{\text{GCT}}$ | $0.245 \cdot 10^{-3}\,\text{V/A}$ |
| Diode D1961 SH45TS02 | | |
| Reverse recov. losses | $e_{\text{rr}}$ | $15.2\,\text{J}$ |
| Diode coefficient | $a_{\text{diode}}$ | $1.19\,\text{V}$ |
| Diode coefficient | $b_{\text{diode}}$ | $0.395 \cdot 10^{-3}\,\text{V/A}$ |

Note that even harmonics of QaHWS OPPs are zero, while triplen harmonics are not considered in the optimization problem as they do not drive harmonic currents in a three-phase load in a wye configuration with a floating star point.

However, as shown in [32], the trade-off between harmonic distortions and losses can be improved by dropping the quarter-wave symmetry. By doing so, half-wave symmetric (HWS) OPPs result, meaning that $2d$ switching angles $\boldsymbol{\alpha}_H = [\alpha_1\ \alpha_2\ \ldots\ \alpha_{2d}]^T \in [0,\pi]^{2d}$ are required instead. The optimization problem to compute OPPs with HWS is

$$\begin{aligned} \underset{\boldsymbol{\alpha_H}}{\text{minimize}} \quad & J(\boldsymbol{\alpha_H}) = \textstyle\sum_{n=5,7,\ldots} \frac{a_n^2+b_n^2}{n} \\ \text{subject to} \quad & a_1 = 0 \\ & b_1 = m \\ & 0 \le \alpha_1 \le \alpha_2 \le \ldots \le \alpha_{2d} \le \pi\,, \end{aligned} \tag{2}$$

where the nonzero $a_n$ and $b_n$ Fourier coefficients are

$$a_n = -\frac{2}{n\pi}\sum_{i=1}^{2d} \Delta u_i \sin(n\alpha_i)\,,$$

$$b_n = \frac{2}{n\pi}\sum_{i=1}^{2d} \Delta u_i \cos(n\alpha_i)\,.$$

Note that all even and triplen harmonics are zero with HWS OPPs as well.

### A. Power Losses Calculation for an NPC Converter

A three-level NPC converter with a machine is shown in Fig. 1. In each phase, there are four active switches $S_1$ to $S_4$ with their respective freewheeling diodes $D_1$ to $D_4$, and two clamping diodes $D_5$ and $D_6$. In this work, the switching devices are the integrated-gate-commutated thyristor (IGCT) 5SHY 4045L0004 [35] by Hitachi and the diode D1961 SH45TS02 [36] by Infineon. The parameters of the semiconductor devices at rated maximum values of anode-cathode voltage $v_T = 2.4\,\text{kV}$ and anode current $i_T = 4.5\,\text{kA}$ are given in Table I.

Usually, the losses of the converter are quantified by the switching frequency. However, the placement of the switching angles can significantly affect the losses as these heavily depend on the commutated current at the switching events and between them. For this reason, an analytical calculation of the losses is considered in this work, as shown in the sequel.

Since OPPs exhibit three-phase symmetry, it suffices to calculate the losses in one phase leg of the NPC converter. Additionally, to simplify the computation of the switching losses, the total dc-link voltage $V_{\text{dc}}$ is assumed constant, and the fluctuations of the neutral-point potential small. As a result, the blocking voltage of each semiconductor is half the dc-link voltage $v_T = \frac{V_{\text{dc}}}{2}$, and the losses depend only on the instantaneous value of the commutated current. The phase current $i_x(t)$ with $x \in \{a,b,c\}$, is considered sinusoidal with frequency $f_1$, i.e., $i_x(t) = \sin(2\pi f_1 t - \phi)$, where $\phi$ is the angular displacement between the phase current and voltage.

The IGCTs produce switching (energy) losses $e_{\text{on}}$ and $e_{\text{off}}$ in turn-on and turn-off events, respectively. The switching losses of the IGCTs are assumed linear in the current, i.e.,

$$e_{\text{on}} = c_{\text{on}}\frac{V_{\text{dc}}}{2} i_x\,, \tag{3a}$$

$$e_{\text{off}} = c_{\text{off}}\frac{V_{\text{dc}}}{2} i_x\,, \tag{3b}$$

where the coefficients $c_{\text{on}}$ and $c_{\text{off}}$ are derived from the data sheets, and $i_x$ is the instantaneous current at a switching event.

On the contrary, the diodes have only turn-off losses—also called reverse-recovery losses $e_{\text{rr}}$—which are nonlinear in the current, i.e.,

$$e_{\text{rr}} = c_{\text{rr}}\frac{V_{\text{dc}}}{2} f_{\text{rr}}(i_x)\,, \tag{4}$$

where the function $f_{\text{rr}}(i_x)$ and coefficient $c_{\text{rr}}$ are derived from the data sheets.

The conduction (energy) losses $e_{\text{con}}$ for both IGCTs and diodes are calculated based on the current. The on-state voltage drop is assumed affine in the current

$$v_T = a + b i_x\,, \tag{5}$$

where the parameters $a_{\text{GCT}}$, $b_{\text{GCT}}$, or $a_{\text{diode}}$, $b_{\text{diode}}$, are selected for $a$, $b$, depending on whether the conducting device is an IGCT or a diode, respectively. As a result, the conduction power losses are given by

$$p_{\text{con}} = v_T(i_x) i_x = a i_x + b i_x^2\,, \tag{6}$$

and the conduction energy losses are

$$e_{\text{con}} = \int p_{\text{con}}\,\mathrm{d}t = \int a i_x(t) + b i_x^2(t)\,\mathrm{d}t\,. \tag{7}$$

For the detailed computation of the losses, the reader is referred to [37, Section 2.3].

Depending on the polarity of the current and the switching transition, different devices turn on and off. The switching losses for a phase leg of an NPC converter are reported in Table II. Similarly, depending on the polarity of the current and the switch position, different devices conduct the current.

TABLE II: Switching energy losses in an NPC phase leg.

| Polarity of phase current $i_x$ | Switching transition | Switching energy losses |
|---|---|---|
| $> 0$ | $0 \to 1$ | $e_{\text{on},S_1} + e_{\text{rr},D_5}$ |
| | $1 \to 0$ | $e_{\text{off},S_1}$ |
| | $0 \to -1$ | $e_{\text{off},S_2}$ |
| | $-1 \to 0$ | $e_{\text{on},S_2} + e_{\text{rr},D_4}$ |
| $< 0$ | $0 \to 1$ | $e_{\text{off},S_3}$ |
| | $1 \to 0$ | $e_{\text{on},S_3} + e_{\text{rr},D_1}$ |
| | $0 \to -1$ | $e_{\text{on},S_4} + e_{\text{rr},D_6}$ |
| | $-1 \to 0$ | $e_{\text{off},S_4}$ |

TABLE III: Conduction energy losses in an NPC phase leg.

| Polarity of phase current $i_x$ | Switch position | Conduction energy losses |
|---|---|---|
| $> 0$ | $1$ | $e_{\text{con},S_1} + e_{\text{con},S_2}$ |
| | $0$ | $e_{\text{con},S_2} + e_{\text{con},D_5}$ |
| | $-1$ | $e_{\text{con},D_3} + e_{\text{con},D_4}$ |
| $< 0$ | $1$ | $e_{\text{con},D_1} + e_{\text{con},D_2}$ |
| | $0$ | $e_{\text{con},S_3} + e_{\text{con},D_6}$ |
| | $-1$ | $e_{\text{con},S_3} + e_{\text{con},S_4}$ |

The conduction losses for a phase leg of an NPC converter are reported in Table III.

In this work, both switching and conduction losses are taken into account. The total power losses of each semiconductor device are the average of the switching and conduction energy losses over the whole fundamental period $T_1 = 1/f_1$, i.e.,

$$P_{\text{tot},z} = \frac{\overbrace{\sum e_{\text{on},z} + e_{\text{off},z}}^{P_{\text{sw},z}}}{T_1} + \frac{\overbrace{\sum e_{\text{con},z}}^{P_{\text{con},z}}}{T_1}, \ \forall z \in \{S_{1,2,3,4}\} \quad (8a)$$

$$P_{\text{tot},w} = \frac{\overbrace{\sum e_{\text{rr},w}}^{P_{\text{sw},w}}}{T_1} + \frac{\overbrace{\sum e_{\text{con},w}}^{P_{\text{con},w}}}{T_1}, \ \forall w \in \{D_{1,2,3,4,5,6}\} \quad (8b)$$

and can be calculated based on the applied OPP, phase current, and displacement angle $\phi$.

Using the above definitions of the switching and conduction losses per device, the maximum losses incurred by a single device are defined as follows

$$P_{\text{max}} = \max\{P_{\text{tot},z}, P_{\text{tot},w}\} \, \forall z \in \{S_{1,2,3,4}\}, w \in \{D_{1,2,3,4,5,6}\} \, . \quad (9)$$

Hence, to find $P_{\text{max}}$, the switching and conduction losses need to be calculated based on the semiconductor switches that commutate the current and the switching events, as described below.

At each switching angle $\alpha_i$, the polarity of the current $i_x(\alpha_i)$ and the corresponding switch positions—namely the switch position $u_{i-1}$ before $\alpha_i$ and $u_i$ after—can be used to determine which devices are turned on and off. For example, if $i_x(\alpha_i) > 0$ and $u_{i-1} = 0$, $u_i = 1$, it can be deduced from Table II that the top outer switch $S_1$ and the upper clamping diode $D_5$ produce turn-on and reverse-recovery losses, respectively, calculated based on (3a) and (4). Hence, using this approach, the switching power losses for each device can be easily computed with the help of (3), (4), and Table II.

Assuming that the current does not change polarity between two consecutive switching angles, $\alpha_i$, and $\alpha_{i+1}$, the conduction losses in that interval are calculated by integrating (6) from $\alpha_i$ to $\alpha_{i+1}$, where the coefficients $a$, $b$ are selected with the help of Table III based on the polarity of $i_x(\alpha_i)$ and the switch position $u_i$. As a sinusoidal current is assumed for the loss calculations, it is implied that its polarity changes at $\phi + k\pi$, $k \in \mathbb{Z}$. Hence, if the subinterval formed by $\alpha_i$ and $\alpha_{i+1}$ does not include a current zero-crossing event, then the conducting devices do not change. As a result, the conduction losses in this subinterval are

$$e_{\text{con}} = \frac{T_1}{2\pi} \int_{\alpha_i}^{\alpha_{i+1}} a i_x(\vartheta) + b i_x^2(\vartheta) \, \mathrm{d}\vartheta \, . \quad (10)$$

If, however, the current changes polarity in the subinterval $[\alpha_i, \alpha_{i+1}]$, i.e., $\alpha_i < \phi < \alpha_{i+1}$, the corresponding conduction losses are computed with the help of two subintegrals, i.e.,

$$\begin{aligned} e_{\text{con}} = &\frac{T_1}{2\pi} \int_{\alpha_i}^{\phi} a_{\text{I}} i_x(\vartheta) + b_{\text{I}} i_x^2(\vartheta) \, \mathrm{d}\vartheta \\ &+ \frac{T_1}{2\pi} \int_{\phi}^{\alpha_{i+1}} a_{\text{II}} i_x(\vartheta) + b_{\text{II}} i_x^2(\vartheta) \, \mathrm{d}\vartheta \, , \end{aligned} \quad (11)$$

where the coefficients $a_{\text{I}}$, $b_{\text{I}}$, and $a_{\text{II}}$, $b_{\text{II}}$ are chosen depending on the conducting devices (see Table III).

### *B. HWS OPP Problem with Limited Power Losses*

Even though conventional OPPs focus on minimizing the load current TDD, they can gain additional features by introducing suitable constraints to the OPP optimization problem. For example, in [38], the computed OPPs also manage to limit the common-mode voltage. Motivated by this, the constraint

$$P_{\text{max}}(\boldsymbol{\alpha_H}, \phi) \leq P_{\text{lmt}} \, , \quad (12)$$

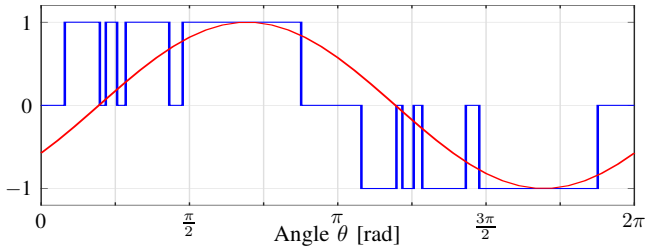
is added to the optimization problem (2) such that loss-constrained OPPs can be computed. In (12), $P_{\text{lmt}}$ is the chosen limit on the total power losses of each switch. Thus, the optimization problem that computes HWS OPPs with bounded power losses is of the form [33]

$$\begin{aligned} \underset{\boldsymbol{\alpha_H}}{\text{minimize}} \quad & J(\boldsymbol{\alpha_H}) = \textstyle\sum_{n=5,7,\ldots} \frac{a_n^2 + b_n^2}{n} \\ \text{subject to} \quad & a_1 = 0 \\ & b_1 = m \\ & 0 \leq \alpha_1 \leq \alpha_2 \leq \ldots \leq \alpha_{2d} \leq \pi \\ & P_{\text{max}}(\boldsymbol{\alpha_H}, \phi) \leq P_{\text{lmt}} \, . \end{aligned} \quad (13)$$

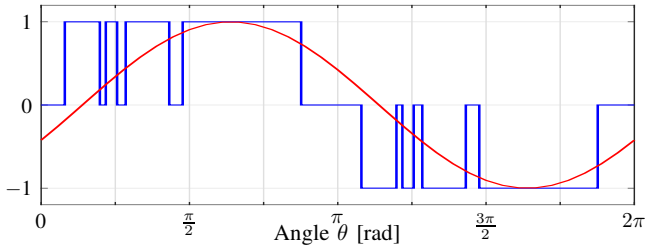
*1) Pulse Dropping:* According to the optimization problem (13), two consecutive switching angles have to meet constraints of the form

$$\alpha_i \leq \alpha_{i+1} \, . \quad (14)$$

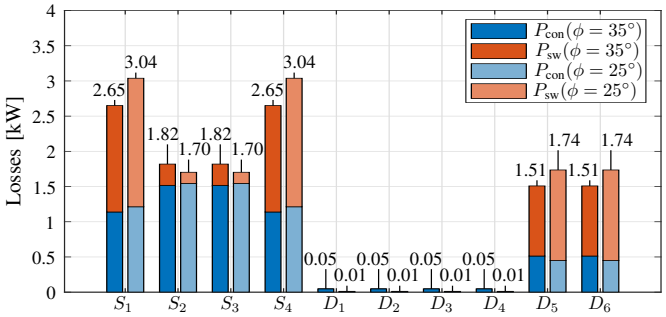
In the corner case $\alpha_i = \alpha_{i+1}$, the two switching transitions cancel each other out, and no switching occurs at $\alpha_i$ (and $\alpha_{i+1}$). This case is referred to as *pulse dropping*. This feature enables the computation of OPPs with $\leq 2d$ switching angles in one half-period when solving the optimization problem for pulse number $d$. This means that if a pattern with $d-1$ pulses can meet the power loss constraint while achieving lower current TDD than any pattern with $d$ pulses, the unnecessary pulses are dropped. This pattern is then returned as the optimal




(a) At $\phi = 35°$ the total losses of $S_1$ are $P_{\text{max}} = 2.65\,\text{kW}$

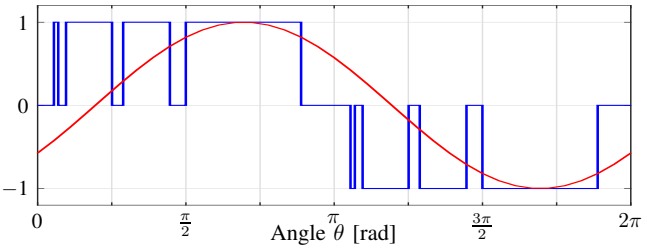



(b) At $\phi = 25°$ the total losses of $S_1$ are $P_{\text{max}} = 3.04\,\text{kW}$

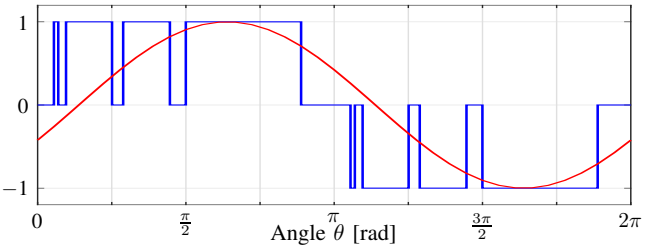



(c) Losses distribution. The switching and conduction losses at $\phi = 35°$ are shown with orange and blue, respectively. The switching and conduction losses at $\phi = 25°$ are shown with light orange and light blue, respectively.

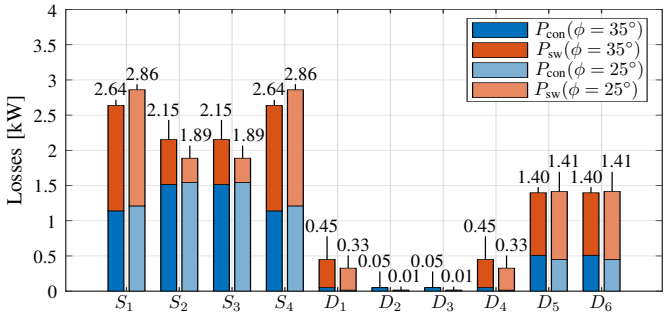
Fig. 2: Loss-constrained HWS OPP (blue) with $d = 4$ and $m = 1.05$, and phase current (red) at different displacement angles. The current TDD produced by this OPP is $I_{\text{TDD}} = 6.58\%$.




(a) At $\phi = 35°$ the total losses of $S_1$ are $P_{\text{max}} = 2.64\,\text{kW}$




(b) At $\phi = 25°$ the total losses of $S_1$ are $P_{\text{max}} = 2.86\,\text{kW}$




(c) Losses distribution. The switching and conduction losses at $\phi = 35°$ are shown with orange and blue, respectively. The switching and conduction losses at $\phi = 25°$ are shown with light orange and light blue, respectively.

Fig. 3: Robust loss-constrained HWS OPP (blue) with $d = 4$ and $m = 1.05$, and phase current (red) at different displacement angles. The current TDD produced by this OPP is $I_{\text{TDD}} = 6.69\%$.

solution without having to solve the optimization problem for $d - 1$ pulses.

However, even though constraint (14) allows for the removal of overlapping switching angles, it does not prevent the occurrence of pulses with infinitesimal width, i.e., in the range of a few $\mu$s. The voltage-second contribution of such pulses, as well as their effect on the current TDD, is insignificant. On the other hand, their presence can lead to significant switching losses. Moreover, such short pulses are not allowed in a physical system, as a minimum on/off time $\Delta t_{\min}$ is required by the devices.

To account for the above, (14) can be modified such that pulses shorter than $\Delta t_{\min}$ are prevented. To this aim, two consecutive switching angles need to have a minimum difference, as dictated by the minimum on/off time $\Delta t_{\min}$. Hence, the following constraint on the switching angles can be considered

$$\alpha_i + 2\pi \frac{\Delta t_{\min}}{T_1} \leq \alpha_{i+1}\,, \tag{15}$$

where $\Delta t_{\min}$ is set to $50\,\mu$s to define the minimum pulse width.

However, the (desirable) pulse-dropping feature is lost when constraint (15) is applied. To overcome this issue, an approach that combines constraint (14) with the minimum pulse width requirement is eventually adopted. More specifically, pulses smaller than $\Delta t_{\min}$ are excluded from the losses calculation process, while the corresponding switching angles that generate such pulses are set equal during the optimization process, i.e., $\alpha_i = \alpha_{i+1}$. This approach retains the pulse-dropping feature, while ensuring that no pattern with pulses shorter than $\Delta t_{\min}$ is considered optimal.

### C. Robust Loss-Constrained OPPs

The total losses of each device vary with the displacement angle $\phi$. As an example, consider the HWS OPP shown in Fig. 2 and the MV drive system with the ratings and parameters mentioned in the beginning of Section IV. When a displacement angle of $\phi = 35°$ is considered (see Fig. 2(a)), this pattern results in $P_{\text{max}} = 2.65\,\text{kW}$, as visualized in Fig. 2(c). However, if the displacement angle changes to $\phi = 25°$ (see Fig. 2(b)), the same OPP will result in $P_{\text{max}} = 3.04\,\text{kW}$. This increase in the maximum losses is due to the narrow pulse occurring at the current zero crossing (at $\theta \approx 35°$) in Fig. 2(a); when the displacement angle changes to $\phi = 25°$ the switching events happen at a higher current, thus generating more switching losses. As a result, the switching losses of the outer switches $S_1$, $S_4$—which are the most stressed devices in the examined scenario—and clamping diodes $D_5$, $D_6$, are

increased while those of the inner switches $S_2$, $S_3$, and outer diodes $D_1$, $D_4$, are decreased, see Fig. 2(c).

Given that the power factor changes during operation, the loss-constrained OPP problem must be solved for multiple displacement angles $\phi$. This approach, however, significantly increases the computational and memory requirements. Therefore, it would be advantageous to compute OPPs that achieve near-optimal performance for a range of operating points. To guarantee that the power losses remain below the desired limit across a range of displacement angles, a modification to constraint (12) is proposed. More specifically, the total losses with $\phi \pm \Delta\phi$, where $\Delta\phi$ is a variation in $\phi$, are also constrained, resulting in the modified constraint

$$\begin{aligned} P_{\text{max}}(\boldsymbol{\alpha}, \phi - \Delta\phi) &\leq P_{\text{lmt}} \text{ and} \\ P_{\text{max}}(\boldsymbol{\alpha}, \phi) &\leq P_{\text{lmt}} \text{ and} \\ P_{\text{max}}(\boldsymbol{\alpha}, \phi + \Delta\phi) &\leq P_{\text{lmt}}\,. \end{aligned} \tag{16}$$

Thus, by replacing constraint (12) with (16) in problem (13), the optimization problem for computing robust loss-constrained OPPs is formulated as

$$\begin{aligned} \underset{\boldsymbol{\alpha_H}}{\text{minimize}} \quad & J(\boldsymbol{\alpha_H}) = \textstyle\sum_{n=5,7,\ldots} \frac{a_n^2+b_n^2}{n} \\ \text{subject to} \quad & a_1 = 0 \\ & b_1 = m \\ & 0 \leq \alpha_1 \leq \alpha_2 \leq \ldots \leq \alpha_{2d} \leq \pi \\ & P_{\text{max}}(\boldsymbol{\alpha_H}, \phi - \Delta\phi) \leq P_{\text{lmt}} \\ & P_{\text{max}}(\boldsymbol{\alpha_H}, \phi) \leq P_{\text{lmt}} \\ & P_{\text{max}}(\boldsymbol{\alpha_H}, \phi + \Delta\phi) \leq P_{\text{lmt}}\,. \end{aligned} \tag{17}$$

By computing OPPs with (17), the variation in losses due to changes in the displacement angle can be reduced. This enhances the robustness of the loss-constrained OPPs, ensuring that the drive utilization is maximized for a given $I_{\text{TDD}}$ over a range of power factors. Finally, it is important to note that the introduction of $\Delta\phi$ affects not only the range of displacement angles over which the OPPs will deliver the desired performance but also the number of LUTs required to store these OPPs. More specifically, a larger $\Delta\phi$ reduces memory requirements but may compromise optimal performance, while a smaller $\Delta\phi$ improves the trade-off between maximum losses per semiconductor device and current TDD at the expense of higher memory consumption. Therefore, $\Delta\phi$ is selected to achieve the best balance between these competing factors.

To illustrate the robustness of these OPPs, a robust loss-constrained HWS pattern with $\phi = 35°$ and $\Delta\phi = 10°$ is considered in Fig. 3. This OPP achieves similar losses in the most stressed device, i.e., $S_1$, as the pattern in Fig. 2 when $\phi = 35°$. Notably, compared to the pattern in Fig. 2, the short pulse is shifted away from the zero crossing of the current. As a result, the increase in the losses of the outer switches is smaller when the pattern is used with a displacement angle of $\phi = 25°$ ($\Delta\phi = 10°$). However, it should be noted that the robustness feature comes at the expense of a slight increase in the current TDD; $I_{\text{TDD}}$ increases from $6.58\%$ to $6.69\%$ in this example, indicating a $1.6\%$ relative increase. Finally, increasing the robustness of OPPs to power factor variations also affects the distribution of the losses among the semiconductor devices, as visualized in Fig. 3(c). The losses of the inner switches ($S_2$ and $S_3$) are closer to those of the outer switches ($S_1$ and $S_4$). Additionally, some of the switching losses shift from the clamping diodes ($D_5$ and $D_6$) to the outer diodes ($D_1$ and $D_4$).

## III. Loss-Constrained OPPs for Displacement Angle $\phi = 35°$

The performance and features of the OPPs in question are discussed hereafter through comprehensive numerical results. All OPPs are computed for an MV drive system consisting of a squirrel cage induction machine with $3.55\,\text{kV}$ rated voltage, $2.2\,\text{kA}$ rated current, $50\,\text{Hz}$ nominal frequency, $0.255$ per unit (p.u.) total leakage reactance, and a three-level inverter with a dc-link voltage of $V_{\text{dc}} = 4.84\,\text{kV}$.

This section compares different types of OPPs in terms of maximum power losses per semiconductor device and $I_{\text{TDD}}$. Specifically, (a) conventional OPPs, i.e., unconstrained QaHWS OPPs computed using problem (1), are compared to (b) loss-constrained HWS OPPs computed with problem (13) and (c) robust loss-constrained HWS OPPs (see problem (17)). For simplicity, OPPs in category "b" are hereafter referred to as lc-HWS OPPs while those in category "c" as rlc-HWS OPPs.

For demonstration purposes, the OPPs are calculated at modulation indices $m = 1$, $m = 1.1$, and $m = 1.2$, and with a displacement angle of $\phi = 35°$, see Figs. 4, 5, and 6, respectively. Note that the modulation index is proportional to the fundamental frequency, with $m = 1.2$ corresponding to the rated voltage. The unconstrained QaHWS OPPs are shown as black asterisks. For the loss-constrained and robust loss-constrained HWS OPPs shown in these figures, only $d = 5$ is considered, while $P_{\text{lmt}}$ varies from $4.5$ to $1.5\,\text{kW}$ in steps of $0.05\,\text{kW}$. The individual lc-HWS OPPs for $d = 5$ are depicted as blue circles, while the corresponding Pareto front is shown with a blue solid line. Finally, rlc-HWS OPPs for $d = 5$ are depicted with a dashed (red) line with triangles.

For example, when considering $m = 1$, as shown in Fig. 4, relaxing the QaHWS to HWS shifts the Pareto front towards the origin. Compared to the unconstrained QaHWS OPP for $d = 2$, this relaxation allows for a reduction in the maximum losses of the most stressed device by up to $0.45\,\text{kW}$, indicating a $19.7\%$ relative improvement, without compromising the current TDD. This results in reduced thermal stress on the semiconductors. Equivalently, when compared with the unconstrained QaHWS OPP for $d = 2$, the $I_{\text{TDD}}$ of the lc-HWS OPPs can be reduced by up to $36.7\%$ without increasing the losses, leading to an improved overall performance and lower thermal losses in the motor.

More impressively, the improved performance compared to the conventional OPPs is not compromised by the addition of the robustness feature. The overall performance of rlc-HWS OPPs is comparable to that of lc-HWS OPPs. Specifically, for the same current TDD, the rlc-HWS OPPs may incur up to $0.07\,\text{kW}$ losses at $\phi = 35°$ when compared to lc-HWS OPPs, which are specifically optimized for that displacement angle. A similar trend is observed for $m = 1.1$, as illustrated in

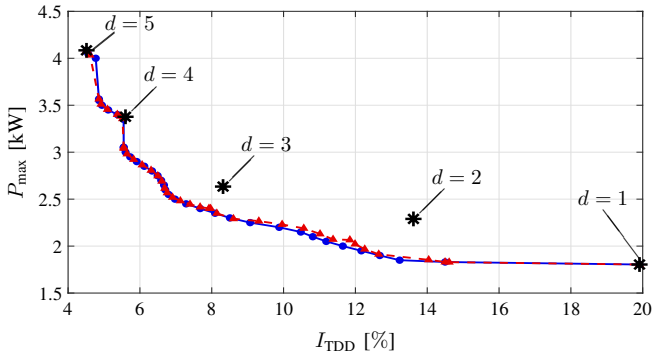



Fig. 4: Maximum power losses per semiconductor device versus current TDD at $m = 1$, and $\phi = 35°$. Conventional QaHWS OPPs are shown with asterisks, lc-HWS OPPs for $d = 5$ are depicted with a solid (blue) line with circles, and rlc-HWS OPPs for $d = 5$ are depicted with a dashed (red) line with triangles.

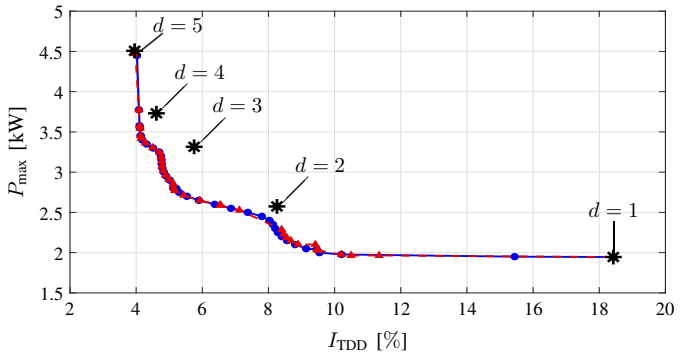



Fig. 5: Maximum power losses per semiconductor device versus current TDD at $m = 1.1$, and $\phi = 35°$. Conventional QaHWS OPPs are shown with asterisks, lc-HWS OPPs for $d = 5$ are depicted with a solid (blue) line with circles, and rlc-HWS OPPs for $d = 5$ are depicted with a dashed (red) line with triangles.

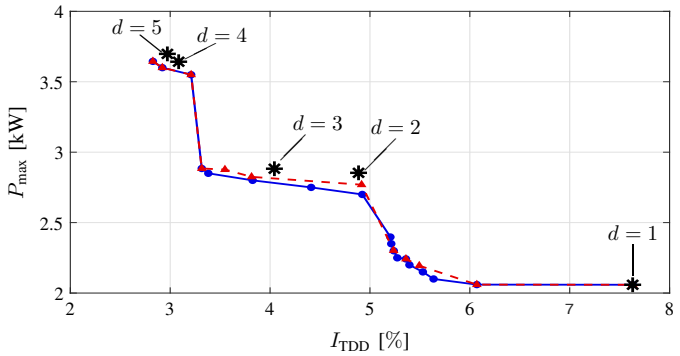



Fig. 6: Maximum power losses per semiconductor device versus current TDD at $m = 1.2$, and $\phi = 35°$. Conventional QaHWS OPPs are shown with asterisks, lc-HWS OPPs for $d = 5$ are depicted with a solid (blue) line with circles, and rlc-HWS OPPs for $d = 5$ are depicted with a dashed (red) line with triangles.

Fig. 5. The proposed rlc-HWS OPPs can reduce the maximum semiconductor device losses by $0.64\,\text{kW}$ compared to the unconstrained QaHWS OPP for $d = 3$, representing a $19.3\%$ relative improvement, while producing the same current TDD. Likewise, the proposed rlc-HWS OPPs can produce similar losses to the unconstrained QaHWS OPP for $d = 3$ while reducing $I_{\text{TDD}}$ by up to $22.6\%$. It is worth noting that the Pareto front of the rlc-HWS OPPs is very close to that of the lc-HWS OPPs. This indicates that also at this modulation index the trade-off between harmonic distortions and power losses remains largely unaffected by the addition of the robustness feature. Similar observations can also be made at the nominal modulation index $m = 1.2$.

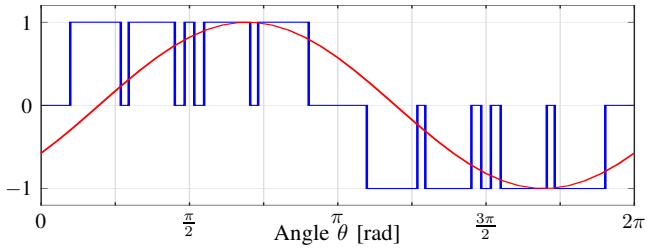
### A. *Pulse Dropping*

For the rlc-HWS OPPs presented in this work, the optimization problem is solved for a single pulse number $d$, and the optimal solution with up to $2d$ switching angles is obtained. This approach offers greater flexibility when higher losses can be tolerated. However, as the upper loss limit becomes tighter, pulses start to drop, implying that the same results could be achieved by initially solving the OPP problem with a smaller pulse number (e.g., $d - 1$). Hence, it suffices to solve the optimization problem with as high a pulse number as possible, as this will yield OPPs with all possible pulse numbers depending on the value of the power loss constraint.

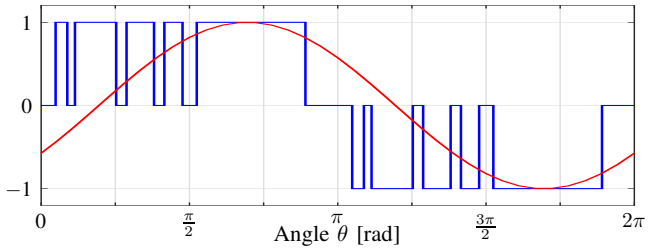
An example of how the patterns change with the upper bound on the losses is illustrated in Fig. 7. More specifically, the conventional OPP for $m = 1$ with pulse number $d = 5$ has $I_{\text{TDD}} = 4.51\%$ and results in maximum losses $P_{\text{max}} = 4.08\,\text{kW}$ in the outer switches $S_1$ and $S_4$ for $\phi = 35°$, see Fig. 7(a). When reducing the upper limit on the losses, the pulses are rearranged within the period so that the switching actions occur at lower current levels, see Fig. 7(b). This adjustment reduces the maximum losses by $1.03\,\text{kW}$, i.e., a $25.2\%$ relative decrease is achieved. However, this comes at the cost of increased current distortions, with a relative increase of $23\%$ in $I_{\text{TDD}}$. The switching and conduction losses of the different patterns at $\phi = 35°$ presented in Fig. 7 are shown in Fig. 7(e) with orange and blue, respectively. As can be seen, when moving from the pattern of Fig. 7(a) to that of Fig. 7(b), the switching losses of the outer switches ($S_1$ and $S_4$) and clamping diodes ($D_5$ and $D_6$) get significantly lower.

As the upper bound on the permissible losses is further reduced, the pulses become narrower and, eventually, some pulses are dropped to reduce the switching losses. For instance, with $P_{\text{max}} = 2.27\,\text{kW}$ (see Fig. 7(c)), the OPP has four pulses, leading to a reduction in maximum device losses by $1.81\,\text{kW}$, i.e., $44.4\%$ relative reduction compared to the unconstrained QaHWS OPP. However, this reduction compromises the current quality as the $I_{\text{TDD}}$ is nearly twice that of the conventional OPP with five pulses. If the limit on the maximum losses per device is further decreased, additional pulses are dropped. To achieve the worst-case losses of $P_{\text{max}} = 1.91\,\text{kW}$, two pulses are dropped, resulting in the pulse number $d = 3$. In this case, the losses of the outer switches are reduced to just $47\%$ of those in the conventional OPP, but the harmonic distortions in the output current are nearly three times higher.

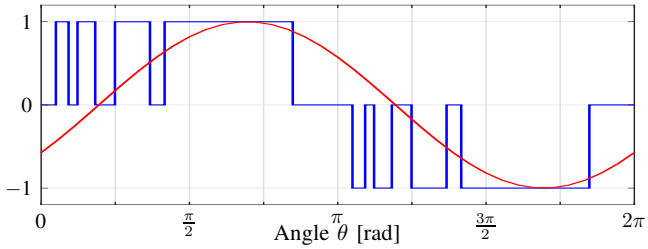
The above results clearly illustrate the trade-off between the maximum losses per semiconductor and the harmonic distortions in the output current. As can be seen, to reduce the losses, the pulses are initially moved closer to the zero crossing of the current. Following, as the loss limit tightens, pulses are dropped to further decrease the switching losses. Finally, it is worth noting that, as shown in Fig. 7(e), the conduction losses remain nearly constant regardless of the limit on the maximum losses. This is because achieving a specific modulation index requires a certain voltage-second contribution.



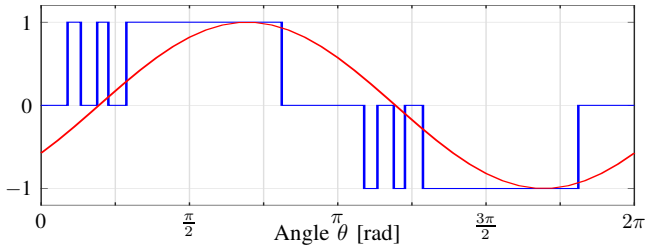

(a) Conventional (unconstrained QaHWS) OPP with $P_{\max} = 4.08\,\text{kW}$ and $I_{\text{TDD}} = 4.51\%$



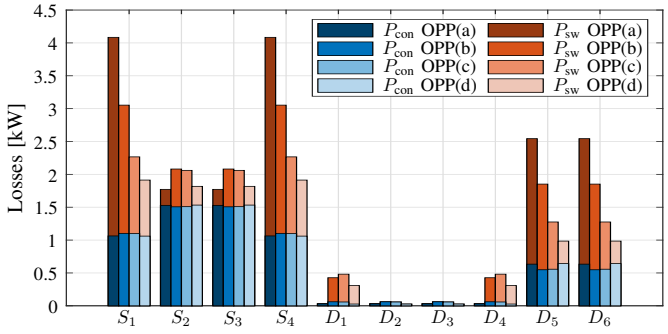

(b) Rlc-HWS OPP with $P_{\max} = 3.05\,\text{kW}$ and $I_{\text{TDD}} = 5.55\%$




(c) Rlc-HWS HWS OPP with $P_{\max} = 2.27\,\text{kW}$ and $I_{\text{TDD}} = 9.31\%$




(d) Rlc-HWS HWS OPP with $P_{\max} = 1.91\,\text{kW}$ and $I_{\text{TDD}} = 12.65\%$

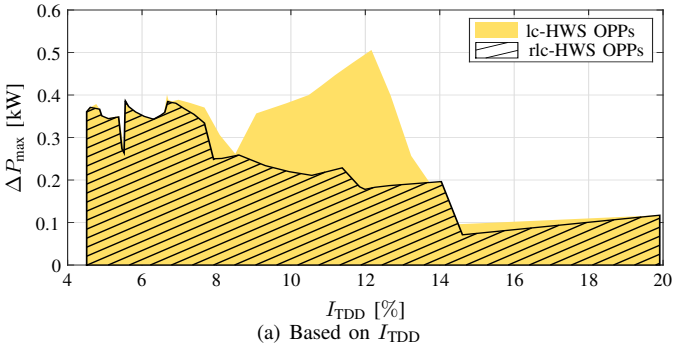



(e) Losses distribution. The switching and conduction losses at $\phi = 35°$ are shown with orange and blue, respectively. The colors from dark to light correspond to the OPPs from (a) to (d), respectively.

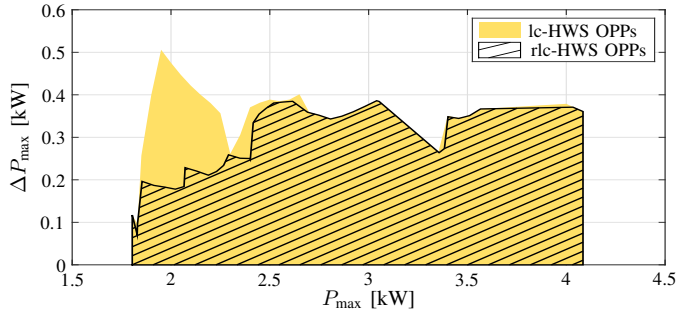
Fig. 7: OPPs with different constraints on the losses for $d = 5$, $m = 1$, and $\phi = 35°$ along with the phase current (red).

### B. Robustness to Power Factor Variations

As demonstrated in Fig. 2, the losses incurred in the switches vary with the change of the displacement angle $\phi$.

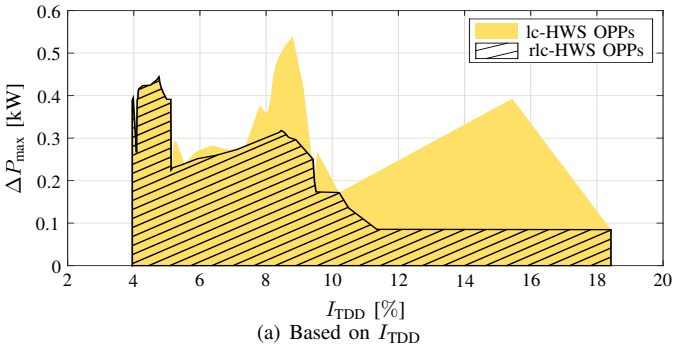



(a) Based on $I_{\text{TDD}}$

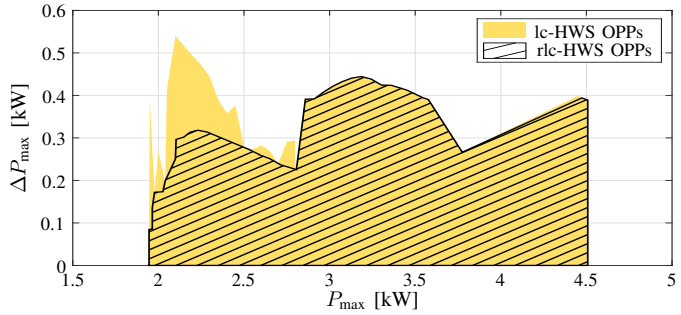



(b) Based on $P_{\max}$

Fig. 8: Maximum absolute variation of the power losses at $m = 1$, $\phi = 35°$ with a changing power factor considering a variation $\Delta\phi = \pm 10°$ of lc-HWS OPPs for $d = 5$ (yellow solid surface) and rlc-HWS OPPs for $d = 5$ (hatched surface).



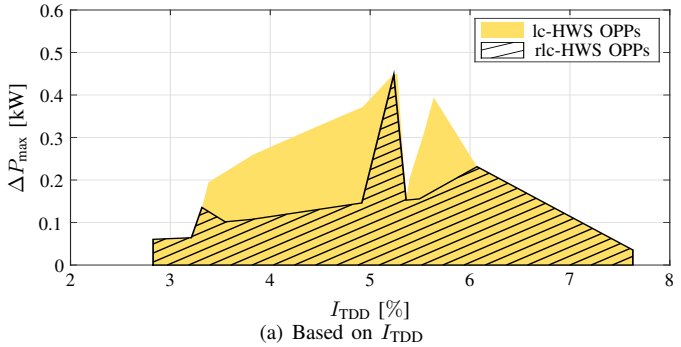

(a) Based on $I_{\text{TDD}}$



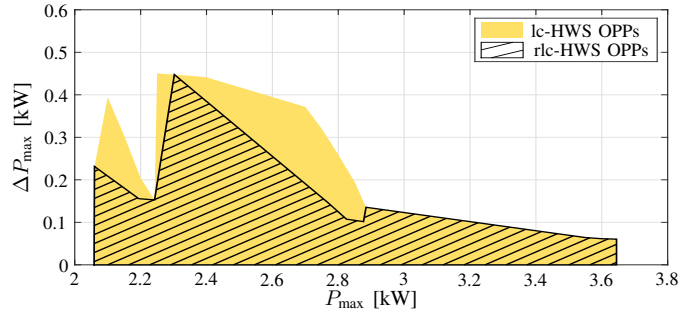

(b) Based on $P_{\max}$

Fig. 9: Maximum absolute variation of the power losses at $m = 1.1$, $\phi = 35°$ with a changing power factor considering a variation $\Delta\phi = \pm 10°$ of lc-HWS OPPs for $d = 5$ (yellow solid surface) and rlc-HWS OPPs for $d = 5$ (hatched surface).

To guarantee that the losses remain within the desired limit across a range of displacement angles, rlc-HWS OPPs should be employed. This approach ensures that the losses of the most stressed device consistently stay below the specified loss limit, while they do not significantly fluctuate with changes in the




(a) Based on $I_{\text{TDD}}$




(b) Based on $P_{\max}$

Fig. 10: Maximum absolute variation of the power losses at $m = 1.2$, $\phi = 35°$ with a changing power factor considering a variation $\Delta\phi = \pm 10°$ of lc-HWS OPPs for $d = 5$ (yellow solid surface) and rlc-HWS OPPs for $d = 5$ (hatched surface).

displacement angle.

To quantify the robustness to the power factor variations, the maximum absolute variation of the maximum losses per semiconductor device, i.e.,

$$\Delta P_{\max} = \max\{|P_{\max}(\varphi) - P_{\max}(\phi)|\}\,,\ \varphi \in [\phi - \Delta\phi, \phi + \Delta\phi] \tag{18}$$

is used as a performance metric. For example, consider the case where $m = 1$, as depicted in Fig. 8. When the permissible losses are high ($P_{\text{lmt}} \geq 2.7\,\text{kW}$), the current TDD remains low ($I_{\text{TDD}} \leq 6.7\%$). In this range, both loss-constrained and robust loss-constrained HWS OPPs result in similar patterns, see Figs. 8(a) and 8(b), and there is no significant improvement in robustness. However, as the constraint tightens, the switching transitions are moved closer to the zero crossing of the current. While this adjustment meets the constraint for a specific displacement angle, it may fail as $\phi$ varies. In contrast, rlc-HWS OPPs favor pulse dropping over narrow pulses, thus improving the robustness as $P_{\max}$ changes from 2.5 to 1.83 kW, corresponding to $I_{\text{TDD}} \in [8\%, 14.5\%]$, as shown in Fig. 8. To achieve $P_{\max} < 1.83\,\text{kW}$, a conventional OPP with $d = 1$ resulting in $P_{\max} = 1.8\,\text{kW}$ and $I_{\text{TDD}} = 19.9\%$ should be used, leaving no OPPs available for $I_{\text{TDD}}$ between $14.5\%$ and $19.9\%$. Similar observations can be made for the rlc-HWS OPPs at different modulation indices, see Fig. 9 for the modulation index $m = 1.1$, and Fig. 10 for $m = 1.2$.

From the presented results it can be concluded that the proposed rlc-HWS OPPs not only reduce the thermal stress on the semiconductor devices for a given $I_{\text{TDD}}$ but are also robust to variations in the power factor. Therefore, this approach ensures converter-friendly operation across a wide range of operating points. However, it should be noted that because the rlc-HWS OPPs are not optimized for a single displacement angle, the trade-off for this advantageous behavior is the potential for slightly higher losses at the nominal angle compared to lc-HWS OPPs tailored to a specific power factor.

## IV. Loss-Constrained OPPs for a Range of Operating Points

This section compares the unconstrained QaHWS OPPs with lc-HWS OPPs and rlc-HWS OPPs across a range of fundamental frequencies, namely $f_1 \in [40, 60]\,\text{Hz}$. Note that since the rated frequency of the machine is 50 Hz, the modulation index is proportional to the fundamental frequency up to that frequency, and it remains constant at its nominal value for $f_1 \geq 50\,\text{Hz}$. As before, the performance is assessed in terms of switching frequency, maximum power losses per semiconductor, and current TDD.

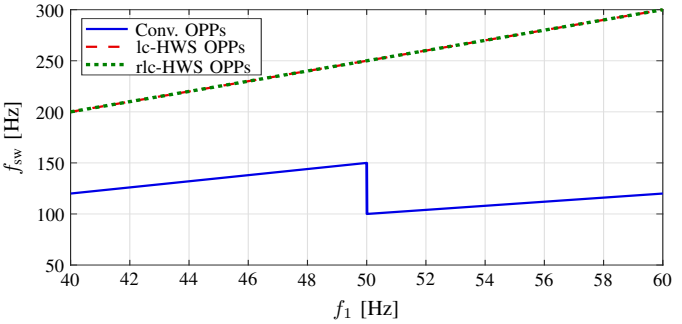
### A. Bounded Maximum Losses

The classic approach to keeping the switching losses low involves limiting the switching frequency below an upper bound $f_{\text{sw,max}}$. The pulse number $d$ is then selected as a function of the fundamental frequency $f_1$, i.e.,

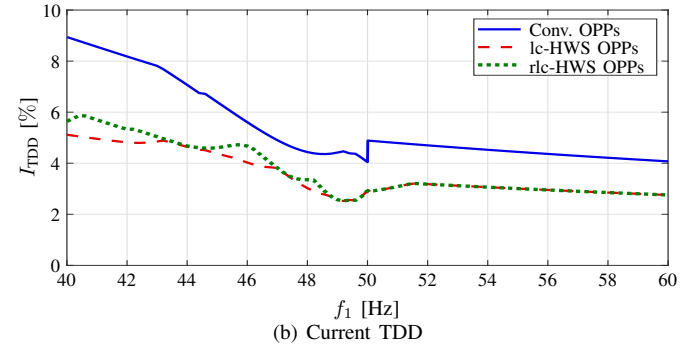
$$d = \text{floor}(f_{\text{sw,max}}/f_1)\,. \tag{19}$$

Considering $f_{\text{sw,max}} = 150\,\text{Hz}$, Fig. 11(a) shows the resulting switching frequency for the aforementioned range of fundamental frequencies. The current TDD and maximum losses per device using conventional unconstrained QaHWS OPPs are illustrated in Figs. 11(b) and 11(c), respectively. As can be observed, there is a noticeable jump in the current TDD at $f_1 = 50\,\text{Hz}$, which is due to the change in the pulse number from $d = 3$ to $d = 2$ occurring at that frequency. Regarding the losses, they vary with the fundamental frequency, with the maximum value within this range of $f_1$ being $P_{\max} = 3.6\,\text{kW}$ at $f_1 = 49\,\text{Hz}$. It is important to note that the maximum losses depend on the modulation index. For instance, the significant drop in the losses after $f_1 = 49\,\text{Hz}$ is attributed to a discontinuity in the switching angles of QaHWS OPPs at the modulation index $m = 1.17$, corresponding to $f_1 = 49\,\text{Hz}$. Due to this discontinuity, the switching angles are redistributed so, combined with the considered displacement angle of $\phi = 35°$, the switching events occur at lower currents, resulting in lower losses.

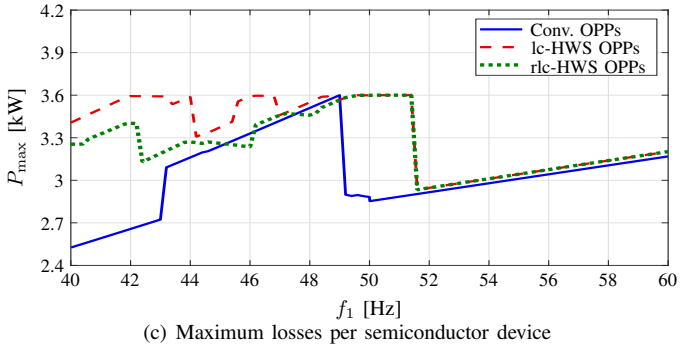
From the above, it can be deduced that the classic approach underutilizes the semiconductor devices. For instance, the maximum losses per device are well below the maximum value of $P_{\max} = 3.6\,\text{kW}$ for most values of $f_1$. To fully utilize the semiconductor devices and enable operation at the maximum permissible power losses, loss-constrained or robust loss-constrained HWS OPPs could be employed. By solving the associated optimization problem for $d = 5$ and $P_{\text{lmt}} = 3.6\,\text{kW}$—matching the maximum losses of the conventional approach with $f_{\text{sw,max}} = 150\,\text{Hz}$—the harmonic performance can be significantly improved while guaranteeing the same worst-case losses for all fundamental frequencies of interest. As shown in Fig. 11(b), with both lc-HWS OPPs and rlc-HWS OPPs the current TDD is reduced by up to $43\%$ compared to



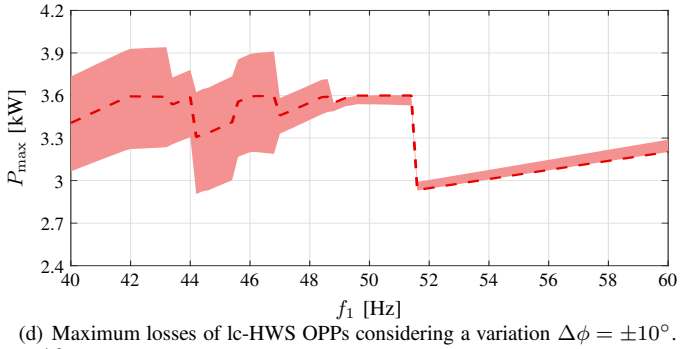

(a) Switching frequency



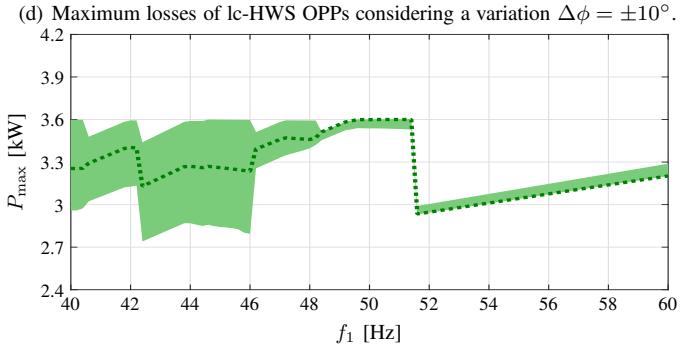

(b) Current TDD




(c) Maximum losses per semiconductor device




(d) Maximum losses of lc-HWS OPPs considering a variation $\Delta\phi = \pm 10°$.




(e) Maximum losses of rlc-HWS OPPs considering a variation $\Delta\phi = \pm 10°$.

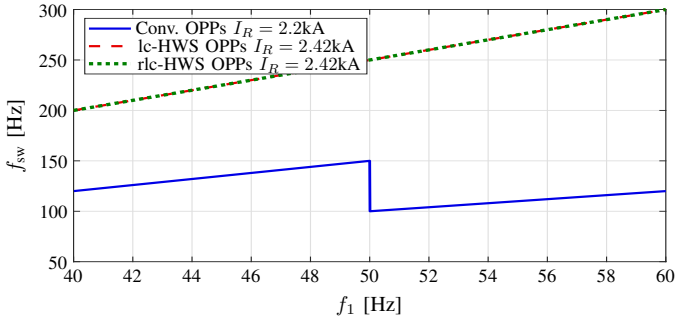
Fig. 11: Classic approach with $f_{sw,max} = 150\,\text{Hz}$ (blue solid line), loss-constrained (red dashed line) and robust loss-constrained (green dotted line) HWS OPPs for $d = 5$ over a range of fundamental frequencies at $\phi = 35°$.

the conventional approach without imposing additional stress on the switches. This significant improvement is largely due to the fact that the proposed OPPs enable operation at much higher switching frequencies than the conventional method, as depicted in Fig. 11(a).

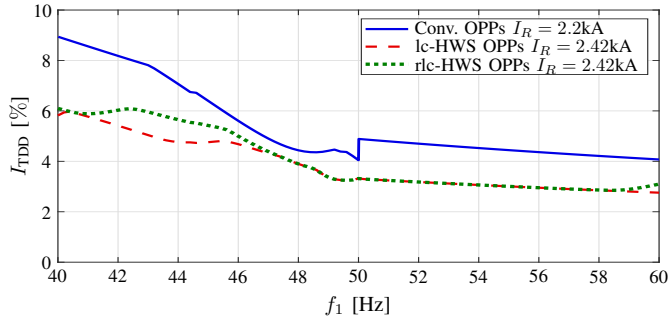
However, when considering a variation of $\Delta\phi = \pm 10°$ in the displacement angle, the maximum losses of lc-HWS OPPs significantly exceed the desired limit of 3.6 kW, as shown in Fig. 11(d). To mitigate this issue, rlc-HWS OPPs can be used instead. By incorporating variations in the displacement angle into the optimization problem, the proposed OPPs produce losses that remain within the loss limit even when the displacement angle changes by the aforementioned degree, as demonstrated in Fig. 11(e). Therefore, this approach enables operation at the loss limit over a wider range of $f_1$ and across a wide range of power factors, thereby maximizing the utilization of the thermal capability of the devices. Note, however, that this robustness feature comes at the expense of potentially increased harmonic distortions. As shown in Fig. 11(b), rlc-HWS OPPs can result in up to 16% higher current TDD compared to lc-HWS OPPs.

### *B. Increased Output Current*

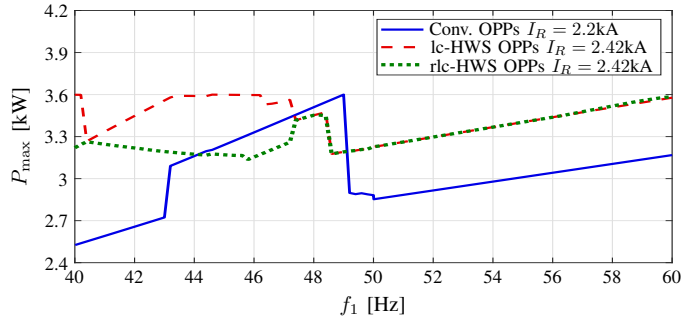
A significant advantage of being able to operate the semiconductor devices at their loss limit without violating it is the potential to increase the rated current. To demonstrate this, the loss-constrained and robust loss-constrained HWS OPP problem is solved assuming a 10% higher stator current, i.e., $I_R = 2.42\,\text{kA}$, with the load inductance adjusted to maintain its p.u. value. The limit on the maximum losses per semiconductor device is kept the same as before, i.e., $P_{lmt} = 3.6\,\text{kW}$. As can be seen in Fig. 12, with the proposed approach, the output rating of the converter can be increased without imposing any additional stress on the semiconductor devices. Specifically, even though the current is higher, it is evident that the maximum losses do not exceed those of the conventional approach with $I_R = 2.2\,\text{kA}$, see Fig 12(c). Additionally, the robustness feature of the proposed method ensures that the worst-case losses remain below the upper limit even when the power factor changes, as seen in Fig. 12(e). More impressively, the harmonic performance is improved compared to the conventional approach across the whole range of fundamental frequencies considered. As depicted in Fig. 12(b), the current TDD is up to 32% lower than in the conventional approach. It is important to note that without the robustness feature, the maximum reduction in current TDD compared to the conventional approach would be 35.5%. However, when considering varying load conditions, the losses would exceed the desired limit, as shown in Fig. 12(d), which makes the lc-OPPs unsuitable for a wide range of operating conditions. This emphasizes the critical advantage of incorporating robustness into the OPPs proposed in [33], ensuring consistent performance and keeping losses within safe limits across different load conditions. Hence, the proposed rlc-HWS OPPs not only improve the harmonic performance while guaranteeing the same worst-case thermal stress as the classic approach but also enable an increase in



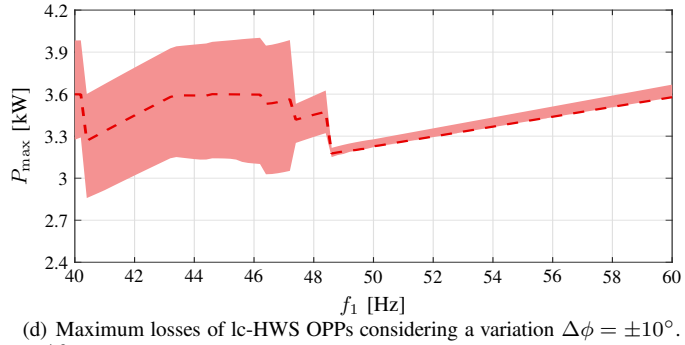

(a) Switching frequency



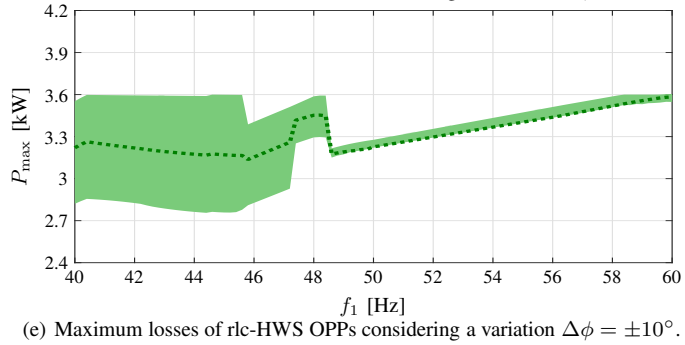

(b) Current TDD




(c) Maximum losses




(d) Maximum losses of lc-HWS OPPs considering a variation $\Delta\phi = \pm 10°$.




(e) Maximum losses of rlc-HWS OPPs considering a variation $\Delta\phi = \pm 10°$.

Fig. 12: Classic approach with $f_{sw,max} = 150\,\text{Hz}$ and $I_R = 2.2\,\text{kA}$ (blue solid line), loss-constrained (red dashed line) and robust loss-constrained (green dotted line) HWS OPPs for $d = 5$ with 10% higher current over a range of fundamental frequencies at $\phi = 35°$.

the rated power of the semiconductor devices. To increase the rated current of the converter, additional components like the busbars, the electromagnetic compatibility (EMC) filter, etc., might need to be uprated as well.

## V. Conclusion

This paper proposed the computation of OPPs that limit the maximum power losses per semiconductor device and offer robustness to power factor variations. The relaxation of the OPP symmetry properties allows rearranging the switching angles within the fundamental period to achieve switching at low currents, and hence reduce the switching losses. Additionally, the inclusion of power factor variation in the optimization problem ensures that the maximum losses do not vary significantly despite changes in the displacement angle. This results in low losses across a wide range of operating points, without significantly compromising the quality of the output current. Therefore, the proposed OPPs achieve the best balance between memory requirements and performance. As demonstrated by the presented numerical results, they significantly improve the fundamental trade-off between current distortions and power losses, closely matching the performance of loss-constrained OPPs without the robustness feature. Importantly, the proposed OPPs also ensure safe operation of the switches over a wide range of operating points. Finally, these OPPs enable an increase in the rating of the semiconductor devices without imposing any additional thermal stress on them, thus offering significant potential for higher hardware utilization.

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