Predictive Control vs. Linear Control for Current Control of a Single-leg Inverter

Toit Mouton*, Peter Stolze†, Tobias Geyer‡, Males Tomlinson§ and Ralph Kennel¶
*§University of Stellenbosch, Stellenbosch, South Africa
Email: *dtmouton@sun.ac.za, §tomlindm@eskom.co.za
†¶Institute for Electrical Drive Systems and Power Electronics, Technische Universität München, Munich, Germany
Email: †peter.stolze@tum.de, ¶ralph.kennel@tum.de
‡ABB Corporate Research, Baden-Dättwil, Switzerland
Email: ‡t.geyer@ieee.org

***Abstract*—This paper presents a comparison of a predictive control scheme with a linear regulator for current control of a single-leg inverter driving a resistive-inductive load with back-EMF. The comparison is motivated by the fact that in most comparisons the linear regulator is not tuned optimally, i.e. it is just providing a suboptimal result. In this paper an oversampled linear resonant regulator is compared to a regularly sampled deadbeat-like predictive control scheme. Due to the fact that both controllers should be implemented on an FPGA for a first approximation it is assumed that the control outputs can be calculated within one FPGA clock cycle. The future reference values are unknown and — despite this fact — the reference should be tracked as accurately as possible. It will be shown that in general a predictive control formulation leads to one sample delay which must not be confused with the more familiar *calculation delay* for software-based implementations of regularly sampled controller implementations.**

I. Introduction

Model predictive control (MPC) [1], [2] has recently emerged as a promising control methodology for power electronics, with the potential of challenging the dominance of PI-based control loops in the next decade for high-performance applications. MPC for power electronics can be broadly classified into three categories: (i) discrete-valued MPC, i.e. direct MPC *without* a modulator, (ii) continuous-valued MPC *with* a subsequent modulator and (iii) MPC modifying the switching transitions of a pre-computed pulse pattern.

In the literature, MPC has been compared and benchmarked with PI-based controllers with modulators for three-phase systems. Regarding the category of direct MPC, finite control set (FCS) MPC has received considerable attention, due to its conceptual simplicity and versatility [3]. Using a prediction horizon of one step, however, limits its steady-state performance. Specifically, when compared to carrier-based pulse width modulation (CB-PWM) or space vector modulation (SVM), FCS-MPC exhibits higher total harmonic distortions (THD) of the currents, when using the same switching frequency. This was shown for induction motor drive systems with different voltage source inverters, namely for a two-level inverter [4], a three-level inverter [5] and a five-phase two-level inverter [6]. During transients, however, the performance of FCS-MPC is typically superior to the one achieved by control loops based on PI controllers, see e.g. [4], [7]. A comparison of FCS-MPC with SVM for a direct matrix converter is shown in [8].

In contrast to that, direct MPC schemes with very long prediction horizons achieve a superior steady-state performance, outperforming CB-PWM and SVM as shown in [9]–[11] and, in some cases, approaching the steady-state performance of optimized pulse patterns (OPP) [5].

A second alternative is to employ continuous-valued MPC, replacing the PI control loops, but keeping the PWM in place. In a field-oriented controller setting for a permanent magnet machine drive system, a comparison between MPC and a PI controller was performed in [12], showing that MPC outperforms the PI loops during transients.

A third approach relies on pre-computing off-line a set of OPPs [13] and to refine the OPP online so as to achieve fast closed-loop control and disturbance rejection. This approach combines the superior steady-state performance of OPPs in terms of very low current THDs per switching frequency, while achieving effectively deadbeat control performance during transients. This MPC concept was introduced in [14], and experimental results on a five-level medium-voltage drive are reported in [15].

The comparison in this paper between MPC and a linear regulator focuses on the single-phase case. This investigation is motivated by the fact that the linear regulator is often not designed in an optimal way, when comparing linear and predictive controllers.

The paper is organized as follows: Section II gives an

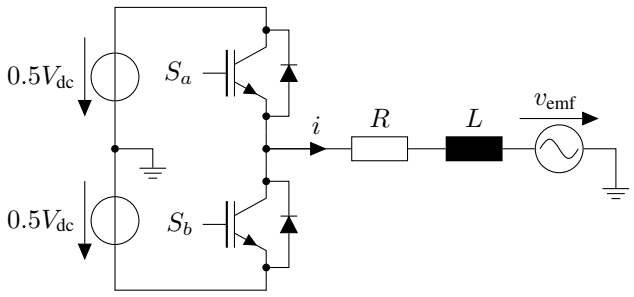

Fig. 1. Physical system

overview of the physical system; in section III the linear control algorithm is described. Section IV provides the predictive control formulations, section V gives an explanation for the delay of predictive control formulations, section VI presents the results of the comparison and in section VII the conclusion and an outlook to further work is given.

II. Physical system and control task

A. Two-level inverter

Fig. 1 shows the single-phase two-level inverter connected to a resistive-inductive load with an (unknown) back-EMF voltage which can be considered as a disturbance. The two switches S_a and S_b are complementary, i.e. if the upper switch is turned *on*, the other one has to be *off* and vice versa. V_{dc} is the DC link voltage and hence, the inverter can produce the voltages $-0.5V_{\text{dc}}$ and $0.5V_{\text{dc}}$. The two switching possibilities are modelled with 1 corresponding to a positive output voltage and -1 for a negative one.

B. Load

The resistive-inductive load with back-EMF is a linear first-order system and can be described by the following differential equation:

$$\frac{\mathrm{d}}{\mathrm{d}t}i = -\frac{R}{L}i - \frac{1}{L}v_{\text{emf}} + \frac{0.5V_{\text{dc}}}{L}s \tag{1}$$

where i is the actual current, v_{emf} is the unknown back-EMF voltage and s is the applied continuous-valued "switching state" which is in the range $[-1 \dots 1]$. The system parameters are the resistor R and the inductor L.

Applying the Euler-forward approximation to equation (1), the following discrete-time system representation can be obtained (sampling interval T_{s}, current time step k):

$$i(k+1) = (1 - \frac{R}{L}T_{\text{s}})i(k) - \frac{T_{\text{s}}}{L}v_{\text{emf}}(k) + \frac{0.5V_{\text{dc}}}{L}T_{\text{s}} \cdot s(k) \tag{2}$$

In order to shorten the expression, equation (2) can be rewritten in the form

$$i(k+1) = a \cdot i(k) + b_1 \cdot s(k) + b_2 \cdot v_{\text{emf}}(k). \tag{3}$$

C. Control task

The control task is to perform current regulation of the given system. A current reference should be tracked as accurately as possible in steady-state as well as during transients. The control scheme should be able to perform this task even if model uncertainties exist, it should be able to reject measurement noise, fluctuations of the DC link voltage and also be able to compensate the back-EMF. Signal propagation delays as well as blanking time should not have significant influence on the control result.

III. Linear regulator

The linear regulator is a highly-oversampled pulse-width-modulated digital current regulator that can be implemented in an FPGA. The sampling frequency is 10 MHz and the control loop is also clocked at this frequency. In [16] it was shown that oversampling results in an increased control bandwidth compared to the conventional regularly sampled digital control loops, while [17] demonstrated that oversampling results in improved transient response. Due to the high oversampling rate of the current regulator it emulates an analog control loop. During the design of analog control loops it is usually assumed that the pulse width modulator is a simple gain block. This assumption results in suboptimal designs. A more accurate model of the pulse width modulator has recently been developed [18]. A brief overview of the design process based on this new model is presented here. A more detailed description of the design procedure as well as experimental results can be found in [19].

Fig. 2 shows the block diagram of the PWM current regulator loop, where $I^{\star}(s)$ is the reference current, $G_c(s)$ is the compensator transfer function and V_d is half the DC bus voltage. The pulse-width modulator is represented by a sawtooth carrier signal $C(s)$ that is subtracted from the modulating waveform followed by a comparator. Delay t_d represents the combined transport delays in the feedback loop. The load back EMF, denoted by EMF(s), is modelled as a disturbance signal. Transfer function $G_p(s)$ represents the RL load and is given by:

$$G_p(s) = \frac{\frac{1}{L}}{s + \frac{R}{L}}$$

In [18] it was shown that the small-signal model of the comparator is a sampling operation followed by an impulse generator with an equivalent small-signal gain K. This gain depends on the slope $\dot{r_0}$ of the comparator input signal just prior to the zero crossings of its input signal and is equal to:

$$K = \frac{2V_d f_s}{|\dot{r_0}|}$$

Fig. 3 shows the small-signal equivalent of the current regulator loop with the pulse-width modulator replaced by this equivalent model. A discrete-time z-domain can be associated with the sampling operation of the pulse-width modulator. The pulse-width modulator essentially samples its reference signal every time the reference intersects the carrier. This discrete-time domain is associated with the short link between the sampler and the impulse generator in the PWM model. The sampling frequency of this discrete-time domain is equal to the switching frequency of the converter. A modified version of the impulse-invariance method [18] is used to transform between the continuous-time s-domain and this z-domain.

The PWM pulse train contains high-frequency ripple components that are injected back into the feedback loop. These ripple components cause an aliasing error during the sampling process as well as a change in small-signal gain due to the gradient of the ripple signal at sampling instances. In most cases this will result in a time-varying reduction of the actual loop gain. In [20] and [21] a simple ripple compensation technique for a single-sided modulator was presented and analysed. The ripple compensation strategy is simply to add the sawtooth carrier to the output of the pulse-width modulator, thereby cancelling the unmodulated edge of the PWM waveform.

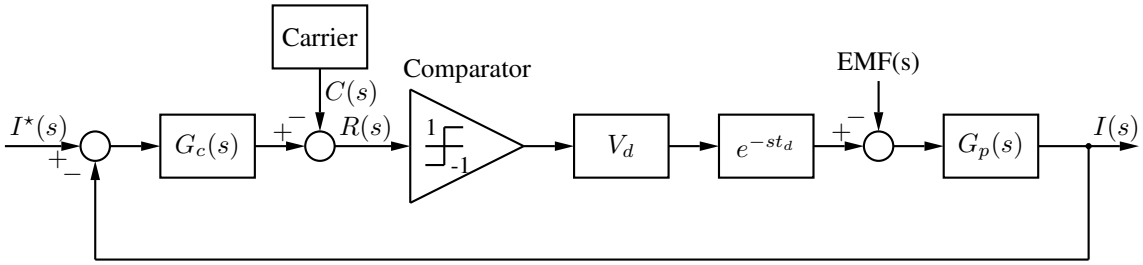

Fig. 2. PWM current regulator loop [19]

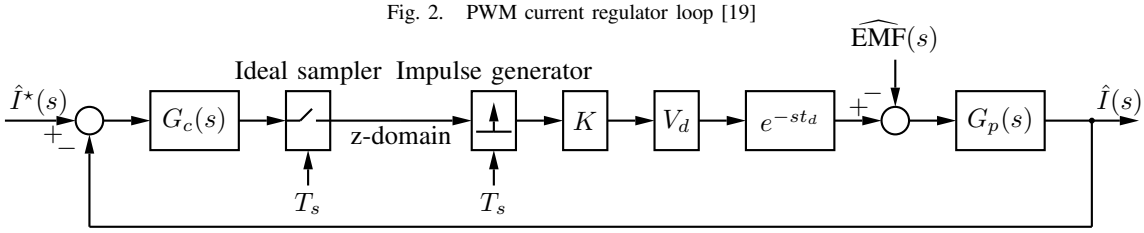

Fig. 3. Current regulator loop z-domain small-signal model [19]

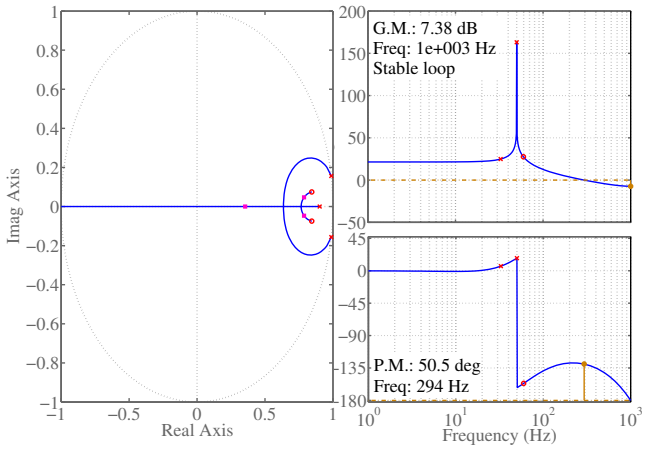

Fig. 4. Current regulator z-domain root locus

Through simple block diagram manipulation it was shown in [21] that this is equivalent to pre-distortion of the carrier. This pre-distorted carrier can be calculated off-line and stored in a lookup table. This strategy solves both problems associated with ripple feedback without limiting the bandwidth of the feedback loop through low-pass filtering.

The approach followed in this paper was to design the feedback compensator directly in the switching frequency z-domain and to then transform the result back to the s-domain to obtain a continuous-time compensator that is implemented in the FPGA. Computational and other delays in the feedback loop of up to one switching period can be compensated for when transforming back to the s-domain. Fig. 4 shows the z-domain root locus of the current regulator. The regulator is designed to accurately track a 50 Hz sinusoidal reference. In theory perfect reference tracking of a 50 Hz reference can be achieved by placing two resonant open-loop poles at 50 Hz on the unit circle. This is similar, but not exactly the same as the PR regulator first proposed in [22].

A slightly modified version of the simple strategy, presented in [23], was used to prevent integrator wind-up during transients.

Unlike the model predictive controller the linear controller does not require any observers to estimate the back EMF. Nor does it require any low-pass filters to remove measurement noise since the compensator acts as a low-pass filter.

IV. Predictive Control Algorithm

The proposed predictive control algorithm uses a deadbeat-like formulation but takes the modulator explicitly into account. A similar approach was presented in [24]. The aim of the controller is to calculate the actuating variable s such that the control error is zero at the *end* of the sample. If the reference cannot be reached by the end of the sample, the controller output will be limited to its maximum or minimum value (1 or -1). For a conventional deadbeat approach the optimum value for the actuating variable s at time step k can be calculated from equation (3) by setting $i(k+1) = i^*$ where i^* is the current reference:

$$s(k) = \frac{1}{b_1} \cdot (i^* - a \cdot i(k) - b_2 \cdot v_{\text{emf}}(k)) \qquad (4)$$

This optimized value then has to be "synthesized" by the modulator since it cannot be produced directly by the inverter. The basic assumption for the modulator is that the *average* voltage applied for one switching state is proportional to the pulse width, e.g. in this case a duty cycle of 50% will lead to an average output voltage of 0 V. For the deadbeat controller this means — assuming again a commanded duty cycle of 50% — that at the *end* of the sample the current will be equal to its reference. However, by taking a look at the system equation (1) it becomes obvious that this assumption is not true — in fact a different value will be obtained.

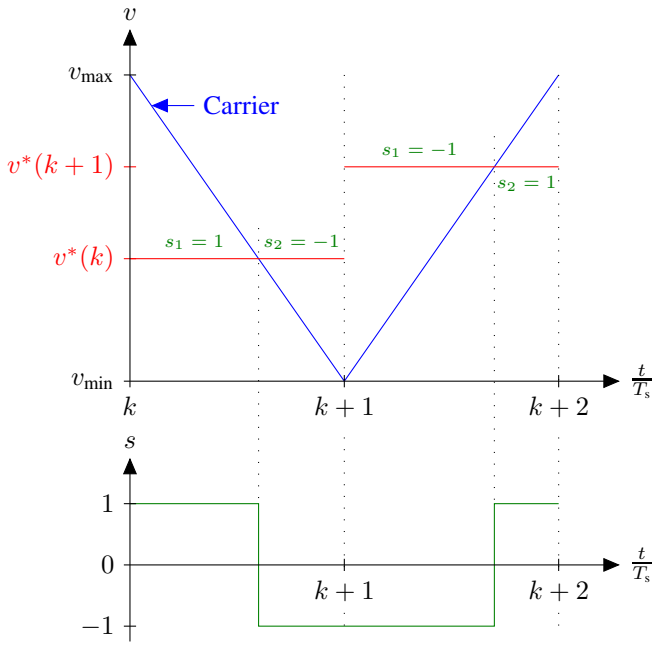

Fig. 5. PWM carrier and applied switching states

Thus, an optimized deadbeat formulation is proposed which corrects the influence of the modulator and calculates an optimized continuous-valued switching state such that the current will in fact be equal to its reference at the end of the sample.

For the controller design it is assumed that a double-edge (triangular) carrier is used whose outputs are visualized in Fig. 5. Since regular sampling is used, the control algorithm will be executed if the PWM carrier is either zero (v_{min}) or at its maximum value (v_{max}). At these points the reference is sampled and the reference voltage for the modulator is calculated (for a first assumption in zero time). For a rising carrier the modulator will output the switching state 1 if the reference is greater than the carrier and -1 vice versa. For a falling carrier, i.e. when the carrier has its maximum value at the beginning of a sample, the first applied switching state will be $s_1 = 1$, the second one $s_2 = -1$; for the case of a falling carrier it is opposite. In the shown example in Fig. 5 the carrier is at its maximum value at time step k, i.e. $s_1 = 1$ will be applied first and then $s_2 = -1$. For the next sample, $k+1$, the carrier is at its minimum value and thus the first applied switching state is $s_1 = -1$; afterwards, $s_2 = 1$ will be applied.

In order to calculate an optimized duty cycle for the controller, it is in the following assumed that the slope of the current does *not* change during one sample, i.e. that it is constant. Fig. 6 shows a simplified graph for one sampling cycle. As already mentioned, the duty cycle p has to be calculated such that the current is equal to its reference at the end of a sample.

In order to obtain the slopes m_1 (for switching state s_1) and

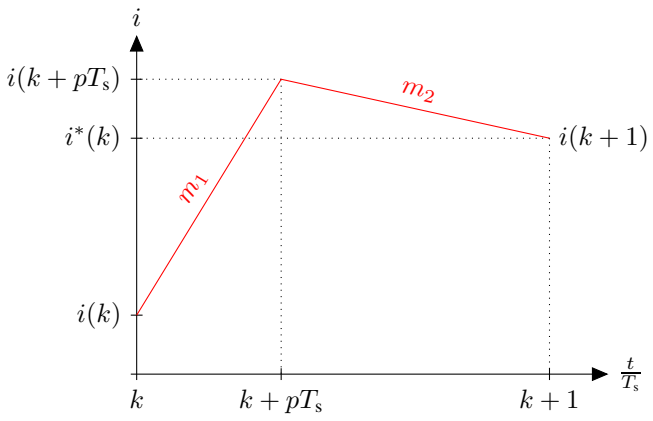

Fig. 6. Optimized duty cycle

m_2 (for s_2), it is assumed that the switching states are applied for one *whole* sample ($i = 1, 2$):

$$m_i = \frac{i(k+1) - i(k)}{T_s} \tag{5}$$

leading to

$$m_i = \frac{(a-1) \cdot i(k) + b_1 \cdot s_i + b_2 \cdot v_{\text{emf}}}{T_s} \tag{6}$$

Then, the optimum duty cycle p (for the switching state s_1 or s_2) can be calculated, assuming that $i(k+1) = i^*$:

$$p = \frac{i^* - i_0 - m_2 T_s}{(m_1 - m_2) T_s} \tag{7}$$

Finally, after some further calculations and replacements, the optimized duty cycle results to

$$p = \frac{i^* - a \cdot i_0 - b_1 \cdot s_2 - b_2 \cdot v_{\text{emf}}}{b_1 \cdot (s_1 - s_2)}. \tag{8}$$

If the output is saturated, i.e. the duty cycle exceeds its allowed range ($[0 \ldots 1]$), it will either be limited to 0 or 1.

It is to be noted that this optimized duty cycle is given for the switching state s_1 which is either 1 or -1 depending if the carrier is rising or falling. Thus, for a rising carrier the duty cycle $1 - p$ has to be commanded to the inverter.

Since a deadbeat control formulation is known to be very sensitive to noise and model imperfections, one possibility to increase its robustness is to put penalties on changes of the control action, i.e. the controller will then react slower to control errors — however, this also results in the fact that it will react slower to reference changes. For the given system a higher prediction horizon (without any penalties on the control action) will finally result in the same controller as a simple deadbeat scheme. Thus, for the given first-order system a higher prediction horizon only makes sense if e.g. penalties on the control action are given. Furthermore, the future values for the next prediction steps are also not known.

In order to improve the control result and to reduce the effect of measurement noise, a simple first-order filter with a cut-off frequency of 100 kHz is used in order to reduce measurement

noise. Since this cut-off frequency is several times higher than the sampling frequency, the filter only leads to a very small delay. Of course, with a higher-order or more sophisticated filter the control result can still be improved.

Due to the fact that a model predictive strategy is used, the back-EMF voltage has to be known, too. One possibility is to use a Luenberger disturbance observer or a Kalman filter [25]. However, it is also possible to calculate the back-EMF from the prediction equations of the previous sample assuming that the back-EMF voltage changes slowly compared to the sampling frequency. In this way a quick and easy back-EMF estimation can be implemented which does not need to be tuned.

Furthermore, it is to be noted that the proposed predictive control scheme does not need any tuning which is an advantage compared to the proposed linear controller.

V. Delay of Predictive Control Formulations

The proposed control algorithm, however, has one significant drawback: In order to track *unknown and time-varying* (e.g. sinusoidal) references accurately and without delay, the reference value at the *end* of the sample has to be known, i.e. the reference value of the *next* sample which still lies in the future. Nevertheless, the controller will deliver an optimal result — however, with *one* sample delay. This problem also occurs for MPC controller formulations.

One possible and commonly known strategy to avoid this delay is reference extrapolation, e.g. with the equation

$$i^*(k+1) \approx 3i^*(k) - 3i^*(k-1) + i^*(k-2). \qquad (9)$$

By applying this strategy, a sine wave or slope can be tracked very well. However, especially for smaller reference steps or if the reference is noisy (e.g. coming from an outer loop) a more sophisticated extrapolation method has to be applied.

VI. Comparison of the Control Algorithms

In order to compare the control algorithms, several simulations have been carried out. The DC link voltage was set to 400 V, the switching frequency was 2 kHz, the model parameters are $L = 17$ mH and $R = 3.5\ \Omega$. The back-EMF voltage is a 50 Hz sine wave with an amplitude of 120 V.

In a first simulation in Fig. 7 the ideal controller behaviour is compared, only a signal propagation delay of the gating signals (500 ns) is assumed. The steady-state tracking error for the predictive control scheme is 2.31 mA, and -1.14° and 0.016 mA and 0.0073° for the linear control scheme.

The second simulations (Fig. 8) show a step response. Due to the extrapolation used by the predictive controller (equation (9)) the reference step shows a delay of one sample. Besides this, the reference is tracked more or less perfectly and without overshoot. The linear controller has almost perfect reference tracking with no delay.

The third simulations, which are shown in Fig. 9, were made in order to investigate the effect of blanking time (5 µs). The steady-state tracking error for the predictive control scheme is 46 mA and -1.26°, and 0.013 mA and 0.00727° for the linear

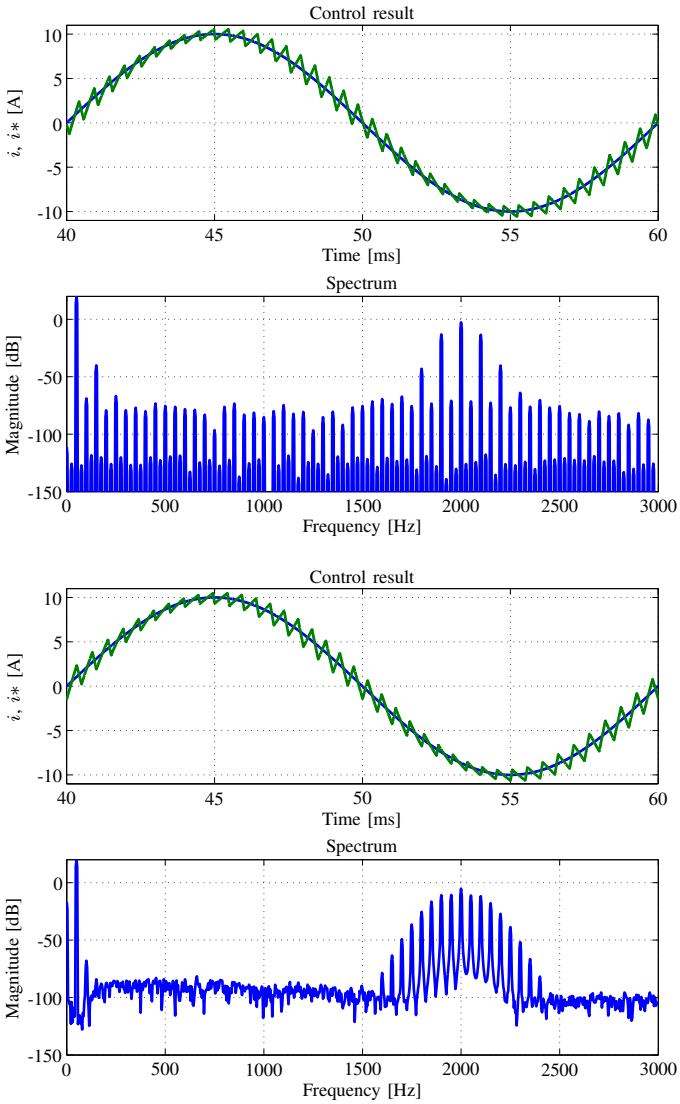

Fig. 7. Sinusoidal current reference tracking. Top: predictive control; Bottom: linear control.

controller. This simulation clearly verifies that the predictive control scheme is much more sensitive to model uncertainties than the linear one.

The fourth simulations which are shown in Fig. 10, were made in order to investigate the effect of measurement noise. The noise was modeled such that it comes close to the typical noise which is produced by compensation-based current measurement devices which are widely used. The steady-state tracking error for the predictive control scheme is 21.95 mA and -1.15°, and 0.083 mA and 0.00741° for the linear controller. Although a low-pass filter was used for the predictive method, in this case the linear controller also delivers much better results.

In order to investigate the effect of DC bus voltage ripple on the control algorithm, an inductor of 0.5 mH and a resistor of 1 Ω were inserted in the positive and negative DC busbars of the converter. The two DC link capacitors each have a

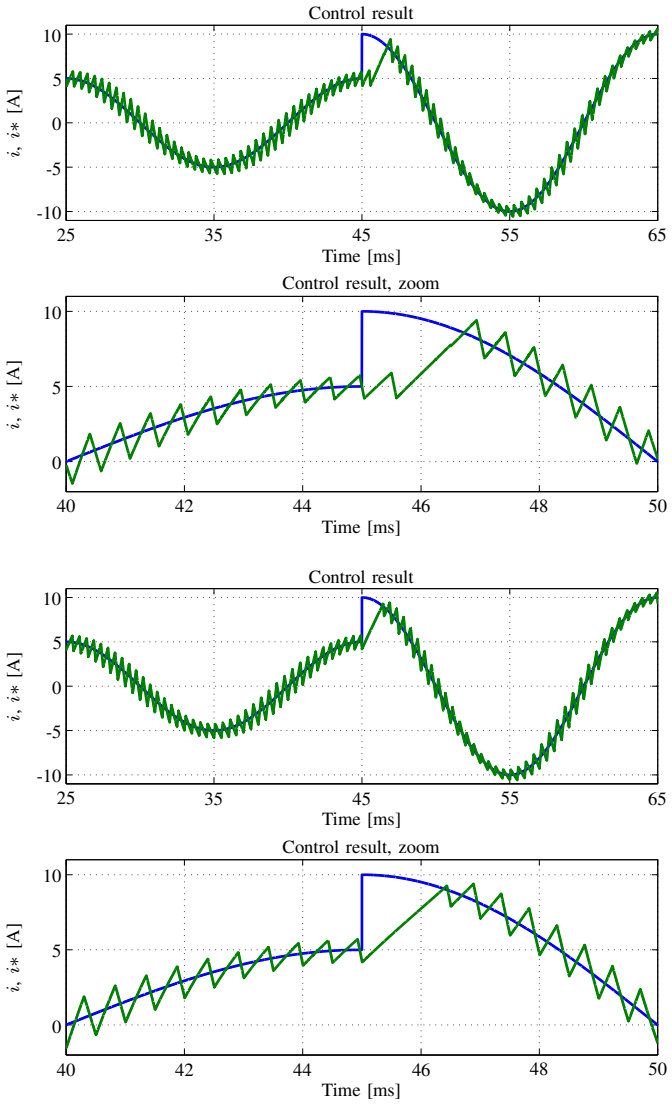

Fig. 8. Step response, Top: predictive control; Bottom: linear control.

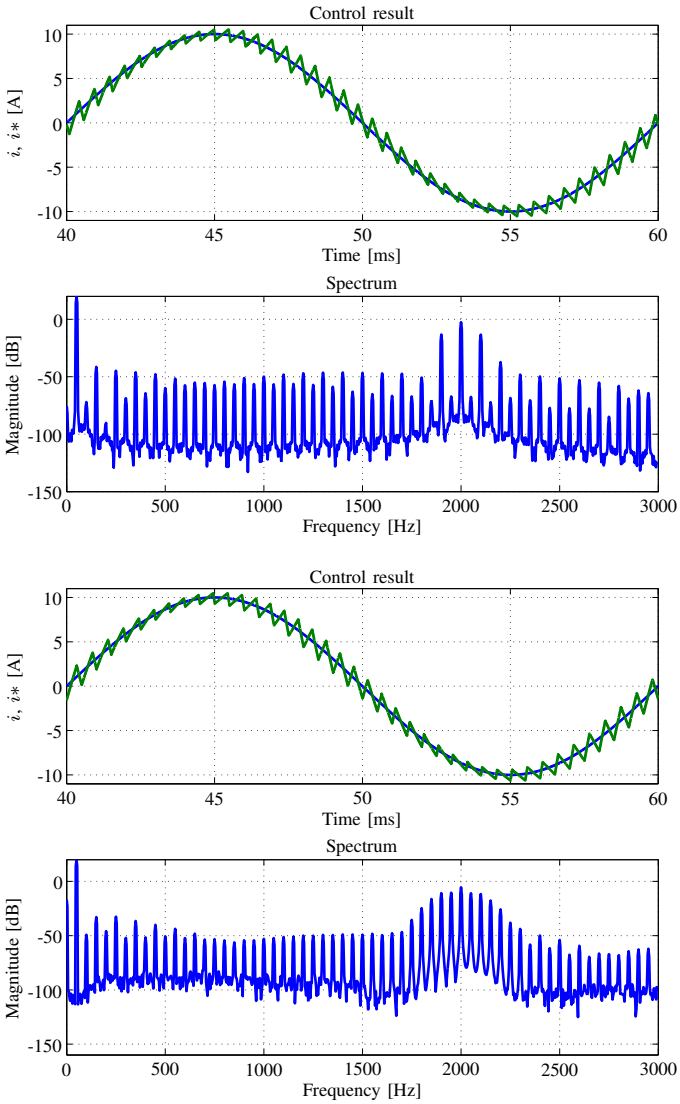

Fig. 9. Effect of blanking time. Top: predictive control; Bottom: linear control.

value of 1 000 µF with an equivalent series resistance of 10 mΩ. This resulted in a voltage ripple of 32 V peak-to-peak across each of the DC link capacitors. The simulation results are shown in Fig. 11. The steady-state tracking error for the predictive control scheme is 29 mA and -1.14°, and 0.0138 mA and 0.00726° for the linear controller. The ripple on the DC bus voltage can be considered as a model uncertainty which deteriorates the control result if a predictive scheme is used. A linear regulator can compensate such uncertainties much better.

The final simulations investigated the sensitivity of the algorithms to model uncertainties. The values of the load inductor and load resistor were halved to 8.5 mH and 1.75 Ω, respectively. The simulation results are shown in Fig. 12. The steady-state tracking error for the predictive control scheme is 346 mA and -1.26°, and 0.029 mA and 0.007° for the linear controller. As the predictive controller is inherently based on a model of the system, model uncertainties have a tremendous effect on the control result. If the system parameters are not well-known, a linear control scheme is clearly superior.

VII. Conclusion and Further Work

In this paper a comparison between an oversampled resonant current regulator and a predictive control scheme was presented. The conducted simulations verify that well-tuned and sophisticated linear controllers can outperform predictive control schemes. Although the linear controller shows a slight undershoot during reference steps, the predictive scheme suffers from the fact that an extrapolation is necessary for an accurate tracking result. If model uncertainties are present (blanking time, measurement noise and changes of the component values), the linear controller delivers much better results than the predictive scheme. One advantage of the predictive controller is that it does not require any (or only little) tuning, i.e. it can quickly be implemented and as long as the system parameters are correct, it will deliver a good

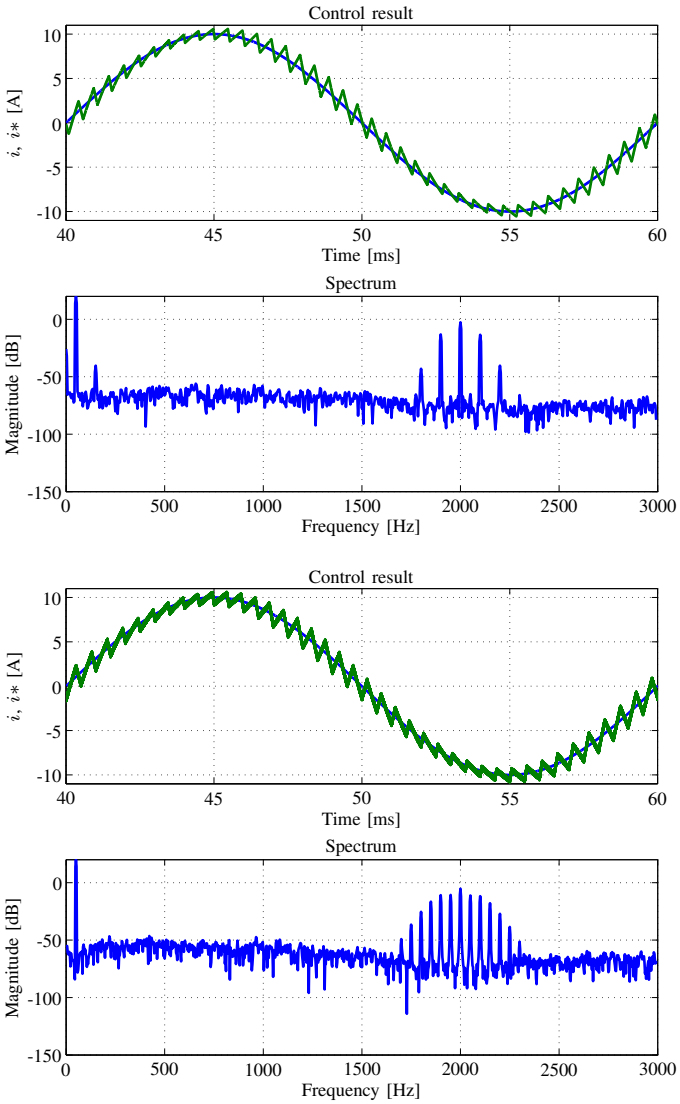

Fig. 10. Effect of measurement noise. Top: predictive control; Bottom: linear control.

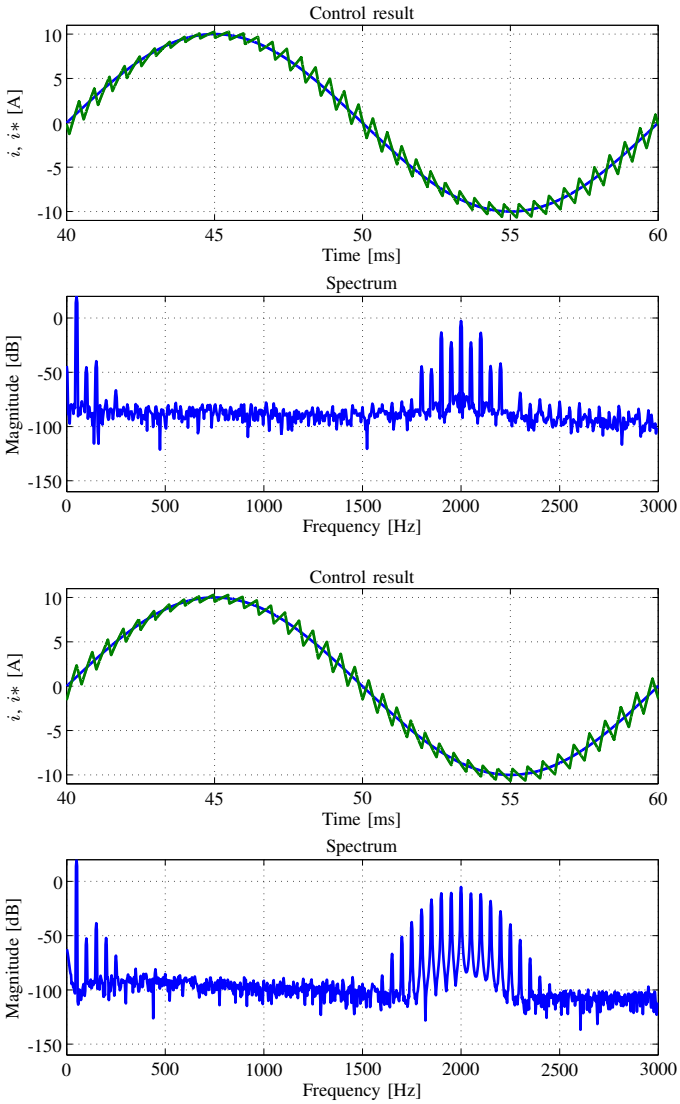

Fig. 11. Effect of DC bus voltage ripple. Top: predictive control; Bottom: linear control.

control result. Finally, it is to be mentioned, that the predictive controller can still be optimized: Besides using a Kalman filter for the current measurements and for the estimated back-EMF, it would also be possible to model the blanking time and DC bus voltage fluctuations. Furthermore, a parameter adaptation algorithm could also be implemented.

REFERENCES

[1] C. E. Garcia, D. M. Prett, and M. Morari, "Model predictive control: Theory and practice—A survey," *Automatica*, vol. 25, no. 3, pp. 335–348, Mar. 1989.

[2] J. B. Rawlings and D. Q. Mayne, *Model predictive control: Theory and design*. Madison, WI, USA: Nob Hill Publ., 2009.

[3] P. Cortés, M. P. Kazmierkowski, R. M. Kennel, D. E. Quevedo, and J. Rodríguez, "Predictive control in power electronics and drives," *IEEE Trans. Ind. Electron.*, vol. 55, no. 12, pp. 4312–4324, Dec. 2008.

[4] J. Rodriguez, R. M. Kennel, J. R. Espinoza, M. Trincado, C. A. Silva, and C. A. Rojas, "High-performance control strategies for electrical drives: An experimental assessment," *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 812–820, Feb. 2012.

[5] T. Geyer, "A comparison of control and modulation schemes for medium-voltage drives: Emerging predictive control concepts versus PWM-based schemes," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1380–1389, May/Jun. 2011.

[6] C. S. Lim, E. Levi, M. Jones, N. A. Rahim, and W. P. Hew, "FCS-MPC-based current control of a five-phase induction motor and its comparison with PI-PWM control," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 149–163, Jan. 2014.

[7] P. Cortés, J. W. Kolar, and J. Rodríguez, "Comparative evaluation of predictive control schemes for three-phase buck-type PFC rectifiers," Harbin, China, Jun. 2012.

[8] M. Rivera, A. Wilson, C. A. Rojas, J. Rodriguez, J. R. Espinoza, P. W. Wheeler, and L. Empringham, "A comparative assessment of model predictive current control and space vector modulation in a direct matrix converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 578–588, Feb. 2013.

[9] T. Geyer and D. Quevedo, "Multistep direct model predictive control for power electronics—Part 1: Algorithm," in *Proc. IEEE Energy Convers. Congr. Expo.*, Denver, CO, USA, Sep. 2013.

[10] ——, "Multistep direct model predictive control for power electronics—Part 2: Analysis," in *Proc. IEEE Energy Convers. Congr. Expo.*, Denver, CO, USA, Sep. 2013.

[11] J. Scoltock, T. Geyer, and U. Madawala, "A comparison of model

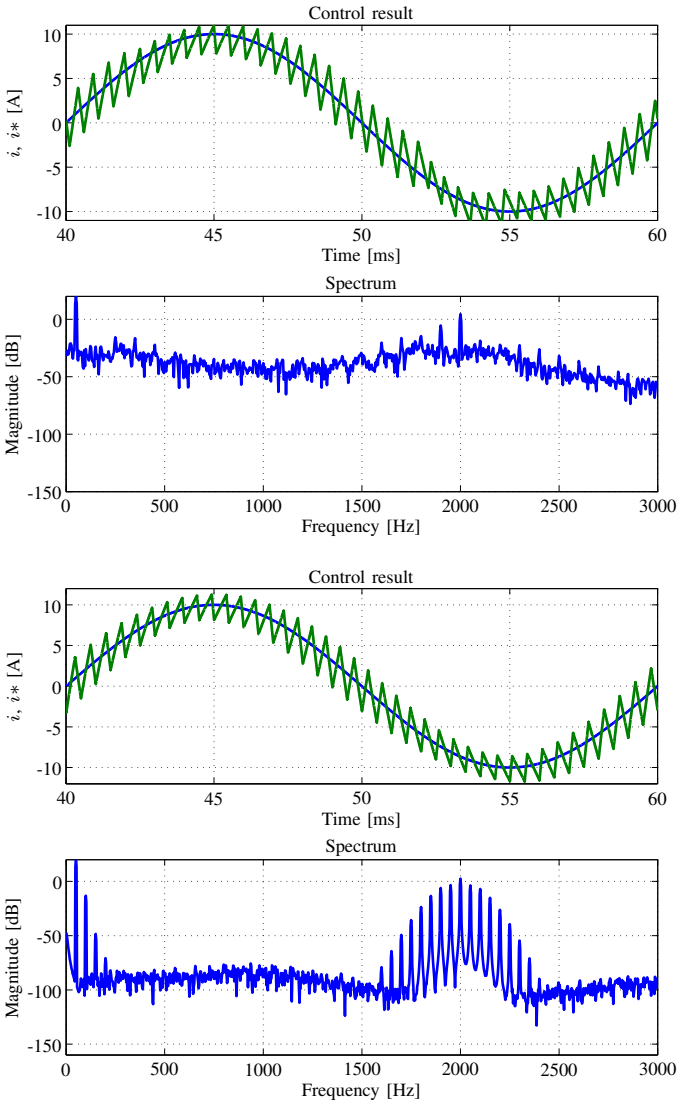

Fig. 12. Effect of changes in component values. Top: predictive control; Bottom: linear control.

predictive control schemes for MV induction motor drives," *IEEE Trans. Ind. Informatics*, vol. 9, no. 2, pp. 909–919, May 2013.

[12] S. Mariéthoz, A. Domahidi, and M. Morari, "High-bandwidth explicit model predictive control of electrical drives," *IEEE Trans. Ind. Appl.*, vol. 48, no. 6, pp. 1980–1992, Nov./Dec. 2012.

[13] G. S. Buja, "Optimum output waveforms in PWM inverters," *IEEE Trans. Ind. Appl.*, vol. 16, no. 6, pp. 830–836, Nov./Dec. 1980.

[14] T. Geyer, N. Oikonomou, G. Papafotiou, and F. Kieferndorf, "Model predictive pulse pattern control," *IEEE Trans. Ind. Appl.*, vol. 48, no. 2, pp. 663–676, Mar./Apr. 2012.

[15] N. Oikonomou, C. Gutscher, P. Karamanakos, F. Kieferndorf, and T. Geyer, "Model predictive pulse pattern control for the five-level active neutral point clamped inverter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Raleigh, NC, USA, Sep. 2012.

[16] L. Corradini, W. Stefanutti, and P. Mattavelli, "Analysis of multi-sampled current control for active filters," in *Industry Applications Conference, 2007. 42nd IAS Annual Meeting. Conference Record of the 2007 IEEE*, sept. 2007, pp. 1608 –1615.

[17] J. Böcker and O. Buchholz, "Can oversampling improve the dynamics of pwm controls?" in *International Conference on Industrial Technology (ICIT)*, Cape Town, South Africa, 2013, pp. 1818–1824.

[18] L. Risbo, "Discrete-time modeling of continuous-time pulse width modulator loops," in *Audio Engineering Society Conference: 27th International Conference: Efficient Audio Power Amplification*, 9 2005. [Online]. Available: http://www.aes.org/e-lib/browse.cfm?elib=13263

[19] T. Mouton, A. de Beer, B. Putzeys, and B. McGrath, "Modelling and design of single-edge oversampled PWM current regulators using z-domain methods," in *ECCE Asia DownUnder*, Melbourne, Australia, June 2013.

[20] B. Putzeys, "Simple, ultralow distortion digital pulse width modulator," in *Audio Engineering Society Convention 120*, 5 2006. [Online]. Available: http://www.aes.org/e-lib/browse.cfm?elib=13498

[21] T. Mouton and B. Putzeys, "Digital control of a PWM switching amplifier with global feedback," in *Audio Engineering Society Conference: 37th International Conference: Class D Audio Amplification*, 8 2009. [Online]. Available: http://www.aes.org/e-lib/browse.cfm?elib=15218

[22] D. Zmood and D. Holmes, "Stationary frame current regulation of pwm inverters with zero steady-state error," *Power Electronics, IEEE Transactions on*, vol. 18, no. 3, pp. 814 – 822, may 2003.

[23] G. Goodwin, S. Graebe, and M. Salgado, *Control system design*. Prentice Hall, 2001. [Online]. Available: http://books.google.co.za/books?id=7dNSAAAAMAAJ

[24] M. Wolf, T. Mouton, and W. van der Merwe, "A low computational double-loop control strategy for dc-ac inverters," in *Southern African Universities' Power Engineering Conference (SAUPEC)*, Johannesburg, South Africa, January 2009.

[25] B. D. O. Anderson and J. Moore, *Optimal Filtering*. Prentice-Hall, Englewood Cliffs, 1979.