Hybrid Modelling and Optimal Control of Switch-mode dc-dc Converters

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Abstract— **This paper presents a new solution approach to the optimal control problem of fixed frequency switch-mode dc-dc converters using hybrid systems methodologies. In particular, the notion of the N-step model is introduced to capture the hybrid nature of these systems, and an optimal control problem is formulated, which allows one to easily incorporate in the controller design safety constraints such as current limiting. The optimal control problem is solved offline resulting in the explicit state-feedback controller that can be stored in a look-up table and used for the practical implementation of the control scheme. Simulation results are provided that demonstrate the prospect of this approach.**

I. Introduction

The problems associated with the analysis and design of the control loop for switch-mode dc-dc converters have attracted a wide research interest, and the quest for efficient control techniques is of interest for both the research and the industrial community. The difficulties in controlling dc-dc converters arise from their hybrid nature. In general, they feature three different modes of operation, where each mode has an associated linear continuous-time dynamic. Furthermore, constraints are present which result from the converter topology. In particular, the manipulated variable (duty cycle) is bounded between zero and one, and in the discontinuous current mode a state (inductor current) is constrained to be nonnegative. Additional constraints may be imposed as safety measures, such as current limiting or soft-starting, where the latter constitutes a constraint on the maximal derivative of the current during start-up. The control problem is further complicated by gross operating point changes due to input voltage and output load variations, and model uncertainties.

In this paper, we focus on fixed-frequency PWM dc-dc converters, where the semiconductor switch is driven by a pulse sequence that has a constant frequency (period), the *switching frequency* f_s (*switching period* T_s), which characterizes the operation of the converter. The dc component of the output voltage can be regulated through the duty cycle d that is defined by $d = \frac{t_{on}}{T_s}$, where t_{on} represents the interval within the switching period during which the switch is in conduction.

Given this principle of operation, the main control objective is to drive the semiconductor switch with a duty cycle such that the dc component of the output voltage is equal to its reference. This regulation needs to be maintained despite variations in the load or the input voltage. The different control techniques that are used in practice have all in common the employment of PI-type controllers that are tuned based on linearized average models [23], [10]. Simple rules are applied, such as selecting a cross-over frequency an order of magnitude smaller than the switching frequency and a phase margin in the range of 45 to 60 degrees.

In the literature, a wide range of different strategies has been proposed for improved controller design. The methods introduced vary from Fuzzy Logic [14] to Linear Quadratic Regulators (LQR) [20], [21], [11], and from non-linear control techniques [24], [25], [16] to feedforward control [17], [18]. The common element in all these approaches is the use of simplified models for the description of the dynamic behavior of switch-mode dc-dc converters. It is obvious that approximations like the use of averaged or locally linearized models do not allow to capture the complex dynamics that stem from the hybrid nature of dc-dc converters, and unavoidably narrow the space of the explored phenomena, thus producing results of limited validity. In particular, for the LQR design in [20], [21] discrete-time models linearized around an operating point are used, and for the nonlinear design in [24], [25], [16] the hybrid nature of the dc-dc converters is bypassed by using an averaged model. Furthermore, none of the proposed controllers allows one to explicitly incorporate constraints in the design procedure.

Motivated by these difficulties, we present in this paper a novel approach to the modelling and controller design problem for dc-dc converters, using a synchronous step-down dc-dc converter as an illustrative example. The converter is modelled as a hybrid system using the Mixed Logic Dynamic (MLD) [4] framework. This leads to a model that is valid for the whole operating regime and captures the evolution of the state variables within the period. Based on the hybrid model, we formulate a finite time optimal control problem, which is solved offline, using Dynamic Programming (DP) [6], producing an explicit state-feedback control law that is parameterized over the whole state-space. This controller can be stored in a look-up table and used for the practical implementation of the proposed control scheme.

The paper is organized in the following way: In Section II, the basic notions that will be used for the hybrid modelling of the converter are introduced. In Section III, the synchronous step-down converter is modelled as a hybrid system by introducing the notion of the N-step model. In Section IV, an optimal control problem incorporating the above mentioned control objectives is formulated. The derivation of the explicit state-feedback control law is treated in Section V. Simulation results illustrating various aspects of the system's behavior are

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given in Section VI. Finally, conclusions and further research directions are discussed in Section VII.

II. Preliminaries on Hybrid Models

The term hybrid systems refers to dynamical systems that contain both analog (continuous) and logical (discrete) components. A number of different subclasses has been introduced for the development of appropriate analysis and design techniques. For the needs of this paper, we focus on two of these subclasses: Mixed Logical Dynamic (MLD) and Piece-Wise Affine (PWA) systems. The MLD formulation is used for the convenient modelling of the converter as a hybrid system, using the compiler HYSDEL (HYbrid System DEscription Language) [27] that produces the matrices of the MLD system starting from a high-level description of the model. Additionally, a PWA representation of the model will be needed at a later stage to precompute offline the explicit state-feedback law for the whole state space that renders the optimal controller applicable for online implementations with sampling times in the range of several μs [7].

A. The Mixed Logical Dynamic Framework

The Mixed Logical Dynamic (MLD) framework is a modelling scheme for discrete-time hybrid systems that is well-suited for optimal control, namely Model Predictive Control (MPC) [22] computations. The general MLD form of a hybrid system introduced in [4] is

$$\mathbf{x}(k+1) = \mathbf{A}\mathbf{x}(k) + \mathbf{B}_1\mathbf{u}(k) + \mathbf{B}_2\boldsymbol{\delta}(k) + \mathbf{B}_3\mathbf{z}(k) \quad \text{(1a)}$$

$$\mathbf{y}(k) = \mathbf{C}\mathbf{x}(k) + \mathbf{D}_1\mathbf{u}(k) + \mathbf{D}_2\boldsymbol{\delta}(k) + \mathbf{D}_3\mathbf{z}(k) \quad \text{(1b)}$$

$$\mathbf{E}_2\boldsymbol{\delta}(k) + \mathbf{E}_3\mathbf{z}(k) \leq \mathbf{E}_4\mathbf{x}(k) + \mathbf{E}_1\mathbf{u}(k) + \mathbf{E}_5\,, \quad \text{(1c)}$$

where $k \in \mathbb{N}$ is the discrete time-instant, and $\mathbf{x} \in \mathbb{R}^{n_c} \times \{0,1\}^{n_\ell}$ denotes the states, $\mathbf{u} \in \mathbb{R}^{m_c} \times \{0,1\}^{m_\ell}$ the inputs and $\mathbf{y} \in \mathbb{R}^{p_c} \times \{0,1\}^{p_\ell}$ the outputs, with both real and binary components. Furthermore, $\boldsymbol{\delta} \in \{0,1\}^{r_\ell}$ and $\mathbf{z} \in \mathbb{R}^{r_c}$ represent binary and auxiliary continuous variables, respectively. These variables are introduced when translating propositional logic or PWA functions into linear inequalities. All constraints on states, inputs and auxiliary variables are summarized in the mixed-integer linear inequality constraint (1c). Note that (1a) and (1b) are linear; the nonlinearity is hidden in the integrality constraints over the binary variables.

We consider MLD systems that are *completely well-posed* [4], i.e. for given $\mathbf{x}(k)$ and $\mathbf{u}(k)$, the values of $\delta(k)$ and $\mathbf{z}(k)$ are uniquely defined by the inequality (1c). This assumption is not restrictive and is always satisfied when real plants are described in the MLD form [4]. Note that the MLD framework allows one to describe automata, propositional logic, $if\ \ldots\ then\ \ldots\ else$ statements and PWA functions. General nonlinear functions, however, can not be modelled, and have to be thus approximated by PWA functions.

B. Piece-Wise Affine Systems

Piece-Wise Affine (PWA) systems [26] are defined by partitioning the state-space into convex polyhedra and associating with each polyhedron an affine state-update and output

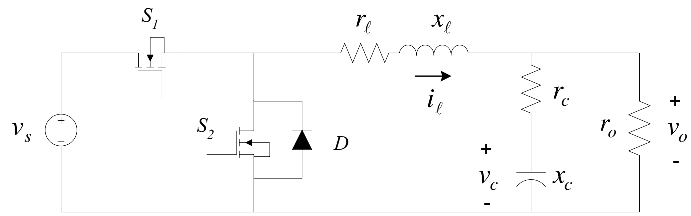


Fig. 1. Topology of the step-down synchronous converter

function

$$\mathbf{x}(k+1) = \mathbf{f}_{j(k)}(\mathbf{x}(k), \mathbf{u}(k)) \quad \text{(2a)}$$

$$\mathbf{y}(k) = \mathbf{g}_{j(k)}(\mathbf{x}(k), \mathbf{u}(k)) \quad \text{(2b)}$$

$$\text{with } j(k) \text{ such that } \begin{bmatrix} \mathbf{x}(k) \\ \mathbf{u}(k) \end{bmatrix} \in \mathcal{P}_{j(k)}, \quad \text{(2c)}$$

where $\mathbf{x}(k)$, $\mathbf{u}(k)$, $\mathbf{y}(k)$ denote at time k the real and binary states, inputs and outputs, respectively, the polyhedra $\mathcal{P}_{j(k)}$ define a set of polyhedra $\{\mathcal{P}_j\}_{j \in \mathcal{J}}$ on the state-input space, and the real time-invariant functions $\mathbf{f}_{j(k)}$ and $\mathbf{g}_{j(k)}$ are affine in the states and inputs, with $j(k) \in \mathcal{J}$, $\mathcal{J}$ finite.

As shown in [15], for a given well-posed MLD model exists always an *equivalent* PWA representation. Equivalence implies, that for all feasible initial states and for all feasible input trajectories, both models yield the same state and output trajectories. Efficient conversion tools are available to transform MLD models into piecewise affine (PWA) models, using the mode enumeration algorithm presented in [12].

III. Modelling the Synchronous Converter

A. Continuous-Time Model

The circuit topology of the synchronous step-down converter is shown in Fig. 1. Using normalized quantities, r_o denotes the output load which we assume to be ohmic, r_c the ESR of the capacitor, r_ℓ is the internal resistance of the inductor, x_ℓ and x_c represent the inductance and the capacitance of the low-pass filtering stage, and v_s denotes the input voltage. For every period k, a duty cycle $d(k)$ which is bounded between zero and one is chosen by the controller. Defining $\mathbf{x}(t) = [i_\ell(t)\ v_c(t)]^T$ as the state vector, the system is described by a set of continuous-time state-space equations of the form

$$\dot{\mathbf{x}}(t) = \begin{cases} \mathbf{F}\mathbf{x}(t) + \mathbf{f}v_s, & kT_s \leqslant t < (k+d(k))T_s \\ \mathbf{F}\mathbf{x}(t), & (k+d(k))T_s \leqslant t < (k+1)T_s \end{cases}, \quad \text{(3)}$$

where the matrices $\mathbf{F}$ and $\mathbf{f}$ are given by

$$\mathbf{F} = \begin{bmatrix} -\frac{1}{x_\ell}(r_\ell + \frac{r_o r_c}{r_o+r_c}) & -\frac{1}{x_\ell}\frac{r_o}{r_o+r_c} \\ \frac{1}{x_c}\frac{r_o}{r_o+r_c} & -\frac{1}{x_c}\frac{1}{r_o+r_c} \end{bmatrix}, \ \mathbf{f} = \begin{bmatrix} \frac{1}{x_\ell} \\ 0 \end{bmatrix} \quad \text{(4)}$$

The output voltage $v_o(t)$ is expressed as a function of the states through

$$v_o(t) = \mathbf{g}^T\mathbf{x}(t) \quad \text{(5)}$$

with

$$\mathbf{g} = \begin{bmatrix} \frac{r_o r_c}{r_o+r_c} & \frac{r_o}{r_o+r_c} \end{bmatrix}^T. \quad \text{(6)}$$

The output variable which is of main interest from a control point of view is the output voltage error which is obtained by integrating the difference between the output voltage and its reference over the k-th switching period, i.e.

$$v_{o,err}(k) = \int_{kTs}^{(k+1)Ts} (v_o(t) - v_{o,ref})\, dt, \qquad (7)$$

where $v_{o,ref}$ denotes the reference of the output voltage.

B. N-step Discrete-Time Hybrid Model

The goal of this section is to derive a model of the synchronous step-down converter that is suitable as a prediction model for the optimal control problem which we will formulate in Section IV. This model should have the following properties. First, it is natural to formulate the model and the controller in the discrete-time domain, as the manipulated variable given by the duty cycle is constant within the period T_s and changes only at every time-instant kT_s, $k \in \mathbb{N}$. Second, it is beneficial to capture the evolution of the states also within one period, as this enables us to impose constraints not only on the states at time-instants kT_s but also on intermediate values. This is particularly important for the inductor current which can vary drastically within one period and would allow us to impose a constraint on its peaks. Third, the model needs to yield an approximation of the output voltage error. Most important, as the converter is intrinsically hybrid in nature, we aim to retain the structure of the two operation modes and account for the hybrid character.

Motivated by these considerations, we introduce the N-step modelling approach that accounts for all the above requested properties by dividing the period of length T_s into N *subperiods* of length $\tau_s = T_s/N$ with $N \in \mathbb{N}$, $N \geq 2$. This concept is illustrated in Fig. 2. We denote the states within a subperiod sampled with τ_s by $\xi(n)$, and we refer to the discrete time-instants of the subperiods by n, where $n \in \{0, 1, \ldots, N-1\}$. Furthermore, by definition, $\xi(0) = x(k)$ and $x(k+1) = \xi(N-1)$.

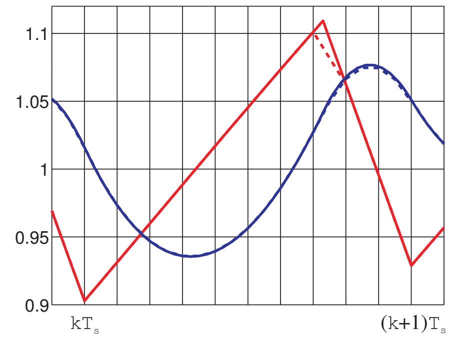
Next, we introduce N binary variables

$$\sigma_n = \text{true} \iff d(k) \geq \frac{n}{N}, \qquad n = 0, \ldots, N-1 \qquad (8)$$

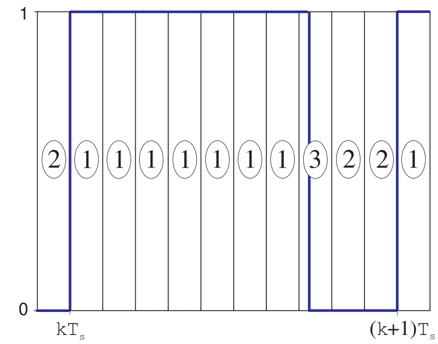
which represent the sampled switch position of S_1 at time-instants $n\tau_s$. Recall that the switch S_2 is dually operated with respect to S_1.

For each subperiod, we introduce the two modes discussed above (switch closed and open, respectively) plus an additional third mode that captures the transition from mode 1 to 2. More specifically, the modes are (i) the switch S_1 remains closed for the whole subperiod, (ii) the switch S_1 is open for the whole subperiod, and (iii) the switch S_1 is opening within the subperiod. Hence, for the n-th subperiod, the state-update equations amount to

$$\xi(n+1) = \begin{cases} \Phi\ \xi(n) + \Psi, & \text{if } \sigma_n \ \wedge\ \sigma_{n+1}, \\ \Phi\ \xi(n), & \text{if } \bar{\sigma}_n, \\ \Phi\ \xi(n) + \Psi(Nd(k) - n), & \text{if } \sigma_n \ \wedge\ \bar{\sigma}_{n+1}, \end{cases} \qquad (9)$$



(a) Evolution of the states



(b) Position of the switch S_1 and the mode which is active in the respective subperiod

Fig. 2. The N-step modelling approach visualized for the k-th period. The evolution of the states of the continuous-time nonlinear model (solid lines) is compared with the sequence of states of the discrete-time hybrid model (dashed lines) using $N = 10$ subperiods, where the saw tooth shaped line represents i_ℓ and the smooth curve is v_c.

where Φ and Ψ are the discrete-time representations of F and f as defined in (4) with sampling time τ_s. The third (auxiliary) mode refers to the mode transition where the switch S_1 opens within a subperiod. Note that if we are in the third mode, i.e. $\sigma_n \ \wedge\ \bar{\sigma}_{n+1}$ holds, $Nd(k) - n$ is bounded by zero and one. Thus, the third mode constitutes a weighted average of modes one and two. The error introduced by averaging can be made arbitrarily small by increasing N.

Using the sampled output voltage given by

$$v_o(n) = g^T\ \xi(n), \qquad (10)$$

we approximate the voltage error integral (7) for the k-th period in the following way.

$$v_{o,err}(k) = \sum_{n=0}^{N-2} \frac{v_o(n) + v_o(n+1)}{2(N-1)} - v_{o,ref} \qquad (11)$$

In summary, the N-step modelling approach provides a description of the state evolution within one period. In particular, the discrete-time sequence of $\xi(n)$, $n = 0, \ldots, N-1$ is an accurate sampled representation of the continuous-time evolution of $x(t)$ for $t \in [kT_s, (k+1)T_s]$. The only approximation that has been introduced appears in the third mode of (9) when the switch S_1 is turned off.

The number N of the subperiods is a design parameter that can be chosen depending on the desired model accuracy. In

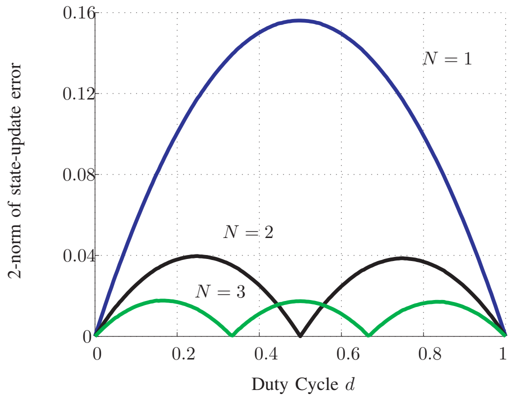


Fig. 3. Accuracy of the state-update of the N-step model

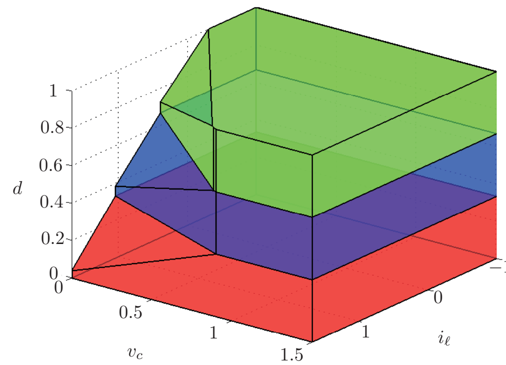


Fig. 4. The polyhedral partition of the converter's PWA model

Fig. 3, the 2-norm of the state-update error of the N-step model is plotted versus the duty cycle for various values of N. The choice of $N = 1$ yields the standard average model that is predominately used for the controller design for dc-dc converters. As one can see, setting $N = 2$ already improves significantly the accuracy of the model.

C. The N-step Model in the MLD Framework

The three modes of the N-step model call for appropriate modelling using hybrid methodologies. Employing the MLD framework described above, one can conveniently model the converter using HYSDEL (HYbrid System DEscription Language) [27]. The derivation of the MLD system is performed by the compiler, which generates the matrices of the MLD system starting from a high-level description. For the N-step model the above procedure yields an MLD system with two states, $7N + 3$ z-variables, N δ-variables and $24N + 18$ inequality constraints.

D. The N-step Model as a PWA System

For the computation of the explicit state-feedback law, it is necessary to transform the N-step model into PWA form. For this, efficient tools are available based on the mode enumeration algorithm presented in [12].

In the case considered, the hybrid model of the converter can be described as a PWA system that is defined over N polyhedra in the state-input space, where N is the number of subperiods used in the previous sections. This partitioning is shown in Fig. 4, where one can observe that the regions are divided along the d axis.

IV. OPTIMAL CONTROL

A. Model Predictive Control (MPC)

Model Predictive Control (MPC) [22] has been used successfully for a long time in the process industry and recently also for hybrid systems. As shown in [4], MPC is well suited for the control of hybrid systems described in the MLD framework. The control action is obtained by minimizing an objective function over a finite or infinite horizon subject to the mixed-integer linear inequality constraints of the MLD model (1) and the physical constraints on the manipulated variables. Depending on the norm used in the objective function, this minimization problem amounts to solving a *Mixed-Integer Linear Program* (MILP) or *Mixed-Integer Quadratic Program* (MIQP).

The major advantage of MPC is its straight-forward design procedure. Given a (linear or hybrid) model of the system, one only needs to set up an objective function that incorporates the control objectives. Additional hard (physical) constraints can be easily dealt with by adding them as inequality constraints, whereas soft constraints can be accounted for in the objective function using large penalties. For details concerning the set up of the MPC formulation in connection with MLD models, the reader is referred to [4] and [2]. Details about MPC can be found in [22].

B. Optimal Control Problem

The control objectives are to regulate the average output voltage to its reference as fast and with as little overshoot as possible, or equivalently, to minimize the output voltage error $v_{o,err}(k)$, despite changes in the input voltage v_s or changes in the load resistance r_o, to achieve operation under a constant duty cycle at steady state, and to respect the safety constraint on the inductor current.

To express these control objectives in a cost function, we introduce the penalties q_1, q_2, q_3 with $q_1, q_2, q_3 \in \mathbb{R}^+$ and define the following costs. First, for the minimization of the output voltage error we set

$$\varepsilon_v(k) = q_1 v_{o,err}(k) \tag{12}$$

Consecutively, in order to induce a steady state operation under a constant duty cycle, we denote with $\Delta d(k) = d(k) - d(k-1)$ the difference between two consecutive duty cycles, and we associate with $\Delta d(k)$ the cost

$$\varepsilon_d(k) = q_2 \Delta d(k) \tag{13}$$

Finally, to account for the bound $i_{\ell,max}$ on the inductor current, we introduce the variable $\varepsilon_i(k)$ that describes the cost of violating this constraint.

$$\varepsilon_i(k) = \begin{cases} 0, & \text{if } i_\ell(k) \leq i_{\ell,max}, \\ q_3(i_\ell(k) - i_{\ell,max}), & \text{else} \end{cases} \quad (14)$$

By associating a large penalty with $\varepsilon_i(k)$, the upper bound on the inductor current is modelled as a soft constraint. (Note that for (14) an additional binary variable is not needed as it can be represented by a slack variable.)

Define the vector $\boldsymbol{\varepsilon}(k) = [\varepsilon_v(k)\ \varepsilon_d(k)\ \varepsilon_i(k)]^T$, and consider the objective function

$$J(\mathbf{D}(k), \mathbf{x}(k), d(k-1)) = \sum_{\ell=0}^{L-1} \|\boldsymbol{\varepsilon}(k+\ell|k)\|_1 \quad (15)$$

which penalizes the predicted evolution of $\boldsymbol{\varepsilon}(k+\ell|k)$ from time-instant k on over the finite horizon L using the 1-norm. The control law at time-instant k is then obtained by minimizing the objective function (15) over the sequence of control moves $\mathbf{D}(k) = [d(k), \ldots, d(k+L-1)]^T$ subject to the mixed-integer linear inequality constraints of the MLD model (1), the physical constraint on the duty cycles

$$0 \leq d(\ell) \leq 1\,, \quad \ell = k, ..., k+L-1 \quad (16)$$

and the expressions (12)–(14). This amounts to the constrained finite-time optimal control problem (CFTOC)

$$\mathbf{D}^*(k) = \arg\min_{\mathbf{D}(k)} J(\mathbf{D}(k), \mathbf{x}(k), d(k-1)) \quad (17a)$$

$$\text{subj. to} \quad (1), (16), (12) - (14), \quad (17b)$$

leading to the sequence of optimal duty cycles $\mathbf{D}^*(k) = [d^*(k), \ldots, d^*(k+L-1)]^T$, of which only the first duty cycle $d^*(k)$ is applied to the converter. At the next sampling interval, k is set to $k+1$, a new state measurement (or estimate) is obtained, and the CFTOC problem is solved again over the shifted horizon according to the receding horizon policy. As we are using the 1-norm in all cost expressions, the CFTOC problem amounts to solving a *Mixed-Integer Linear Program* (MILP) for which efficient solvers exist.

V. The State-feedback Law

In this section, we provide some information regarding the explicit state-feedback controller. More specifically, in Section V-A, we refer to the work that has been done in the development of algorithms for deriving such controllers and highlight some of the fundamental properties of the obtained controller. In Section V-B some implementation issues are briefly discussed.

A. Algorithm and Properties

Recall that the objective function (15) is linear, and rewrite the CFTOC (17) by replacing the MLD model by the equivalent PWA model (2)

$$\mathbf{D}^*(k) = \arg\min_{\mathbf{D}(k)} J(\mathbf{D}(k), \mathbf{x}(k), d(k-1)) \quad (18a)$$

$$\text{subj. to} \quad (2), (16), (12) - (14). \quad (18b)$$

Note that the CFTOC problem is not only a function of the state vector $\mathbf{x}(k)$, but also of the last control move $d(k-1)$, as we are penalizing the changes of the duty cycle in the objective function. The optimal control move for the problem (18) may be obtained by solving a mixed-integer optimization problems online or by solving offline a number of multi-parametric linear programs.

By multi-parametric linear programming, a linear optimization problem is solved offline for a range of parameters. In [5], the authors show how to reformulate a discrete-time CFTOC problem as a multi-parametric program by treating the state vector as a parameter and propose an algorithm for its solution. Basic ideas from [5] for linear systems with quadratic cost are extended in [3] to linear systems with linear cost expressions, and in [1], [9], [19], [7] to PWA systems. The details about the algorithm computing the explicit state-feedback control law can be found in [1], where the authors report an algorithm that generates the solution by combining dynamic programming with multi-parametric programming and some basic polyhedral manipulations.

Next, we restate the main result about the solution to the CFTOC problem (18) proven in [7]. The optimal state-feedback control law $d^*(k)$ is a PWA function of the state $\mathbf{x}(k)$ defined on a polyhedral partition of the feasible state-space. In our case, as the CFTOC is also a function of the last control input, we need to extend the state vector by $d(k-1)$. Furthermore, the value function $J(\mathbf{x}(k), d(k-1)) := J(\mathbf{D}^*(k), \mathbf{x}(k), d(k-1))$ is also PWA in the state and the last control input.

B. Implementation

As a result, such a state-feedback controller can be implemented online, since computing the control input amounts to the following two steps. First, the polyhedron needs to be determined in which the measured state lies. A brute force approach would be to go through (in the worst case the whole) set of polyhedra and to check the corresponding inequalities of the polyhedra. A smarter technique has been proposed in [8] exploiting the properties of the value function.

In general, polyhedra with the same control law form a convex union and can thus be merged and replaced by their union. This leads to an equivalent PWA control law with less polyhedra and thus reduced complexity. Such a representation is highly preferable as it allows one to relax the memory requirements and to reduce the computational burden for the controller hardware. Indeed, it is possible to derive an equivalent PWA control law that is *minimal* in the number of polyhedra by merging polyhedra associated to the same control law in an optimal way [13].

VI. Simulation Results

The results presented here concern initially the explicit state-feedback controller that was derived for the set of converter and control problem parameters provided in Table I. In the sequel, we examine two aspects of the system's dynamic behavior. In the first case, the behavior of the converter during

TABLE I
PARAMETERS USED FOR THE SIMULATION RESULTS

Parameters of the Converter					
x_c	70 p.u.	x_ℓ	3 p.u.	$i_{\ell,max}$	3 p.u.
r_c	0.001 p.u.	r_ℓ	0.05 p.u.	r_o	1 p.u.
Parameters of the Control Problem					
N	3	L	2		
q_1	4	q_2	0.1	q_3	1000 p.u.

start-up is investigated, while in the second case the system's response to changes of the input voltage is examined. The simulations were carried out using the nonlinear model of the converter as the real plant, closing the loop with the explicit state-feedback controller. The states of the converter and the input voltage were regarded to be ideally measurable. All units in the following figures are normalized, including the time scale where one time unit is equal to one switching period.

A. The Explicit State-feedback Controller

As mentioned above, the formulation of the control problem presented here is expected to lead to an explicit state-feedback control law that is defined in a 3-dimensional space. This is due to the fact that the cost function penalizes the changes in the duty cycle and therefore the controller action depends on $d(k-1)$ as well. However, in order to account for changes of the input voltage, one additional parameter needs to be introduced, leading to a 4-dimensional problem. Using a straightforward approach, one could use the input voltage as a parameter in the CFTOC, which would result in a problem of increased complexity, since v_s enters the state-update equations (9) in a nonlinear fashion (multiplied with the duty cycle).

In order to avoid this complexity increase, we use the reference voltage v_{ref} as a parameter instead. For this to be possible, one just needs to norm the measurements acquired at the beginning of each period to the input voltage, and adopt the reference accordingly. Using this strategy, the problem is still 4-dimensional but no additional nonlinearities are introduced. This procedure resulted in a state-feedback controller defined on 325 polyhedral regions in a 4-dimensional space. Using the merging algorithm presented in [13], the controller was simplified to 100 regions. Figure 5 shows a cut through the control law along the control $d(k-1) = 0.5$ and $v_{ref} = 0.556$, where one can observe the control input $d(k)$ as a PWA function of i_ℓ and v_c.

B. Case 1: Start-up

The first case presented in Fig. 6 shows the step response of the converter in nominal operation during start-up. The initial state is given by $x(0) = [0\ 0]^T$, the input voltage is $v_s = 1.8$ p.u. and the reference for the output is $v_{o,ref} = 1$ p.u. The output voltage reaches its steady state within 10 switching periods with an overshoot that does not exceed 3%. The current constraint is respected by the peaks of the inductor current during start-up, and the small deviations observed

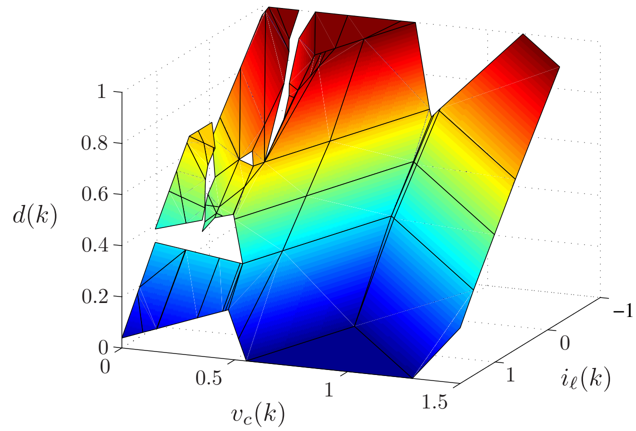


Fig. 5. The state-feedback controller for $d(k-1) = 0.5$ and $v_{o,ref} = 0.556$ p.u

are due to the approximation error introduced by the coarse resolution chosen for the N-step model. The same holds for the small -in the range of 0.5%- steady-state error that is present in the output voltage.

C. Case 2: Response to input voltage changes

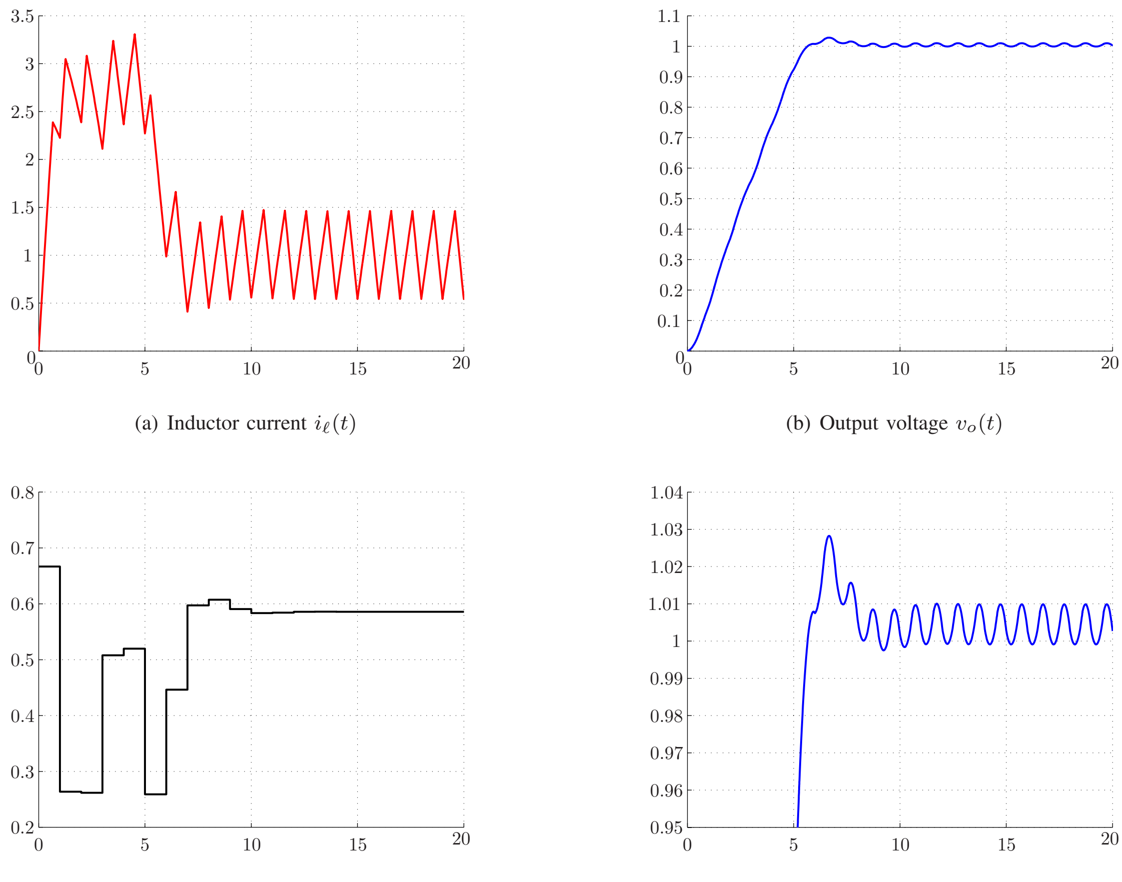
In the second case, we examine the behavior of the converter under step changes in the input voltage. In the examples presented, the converter is initially at steady state when a step change in the input voltage is applied at time-instant $k = 5$.

In the first example shown in Fig. 7, the input voltage changes from $v_s = 1.8$ p.u. to $v_s = 3$ p.u.. As can be seen from Fig. 7, the output voltage remains practically unaffected and the controller finds the new steady-state duty cycle very quickly (within 4 switching periods). In the second example depicted in Fig. 8, the input voltage changes from $v_s = 1.8$ p.u. to $v_s = 1.2$ p.u.. Similar to the previous case, the output voltage remains practically unaffected, and the relatively large undershoot results from the physical limitation of the duty cycle, as can be seen by the graph in Fig. 8(b).

VII. CONCLUSIONS AND OUTLOOK

In this paper, we have presented a new solution approach to the optimal control problem of fixed frequency switch-mode dc-dc converters using hybrid systems methodologies. A novel N-step hybrid model was introduced, and an optimal control problem was formulated and solved offline, yielding an explicit state-feedback controller defined over a polyhedral partition of the state-space that allows for the practical implementation of the proposed scheme. The use of MPC has allowed us to explicitly take into account during the controller design physical constraints, such as the restriction of the duty cycle between zero and one, and safety constraints, such as current limiting. Simulation results have been provided demonstrating that this approach leads to a closed-loop system with very favorable dynamical properties.

However, this study has been so far limited to the case where the states of the converter, namely the inductor current and



(a) Inductor current $i_\ell(t)$

(b) Output voltage $v_o(t)$

(c) Duty cycle $d(t)$

(d) Detail of $v_o(t)$

Fig. 6. Closed-loop simulation of the converter during start-up

the capacitor voltage, are considered to be ideally measurable. This assumption represents a shortcoming that in the course of further research needs to be addressed. Moreover, the issue of the variations of the converter's load has not been addressed in this paper. Nevertheless, the preliminary results that have been obtained show that the proposed scheme can be adopted to handle these variations, without becoming too complex for a practical application.

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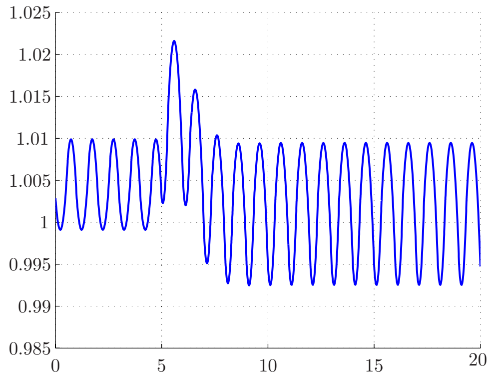
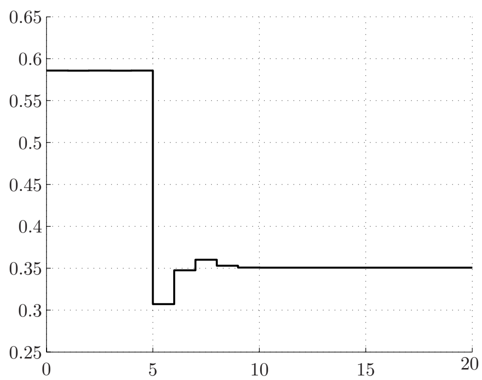
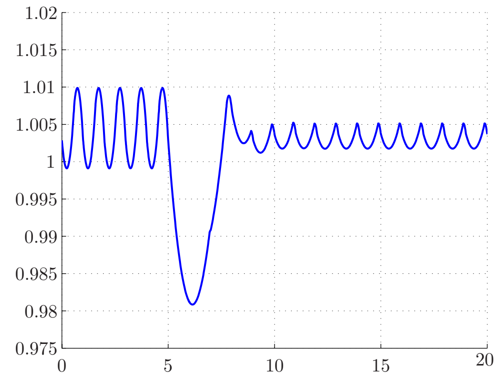


(a) Output voltage $v_o(t)$

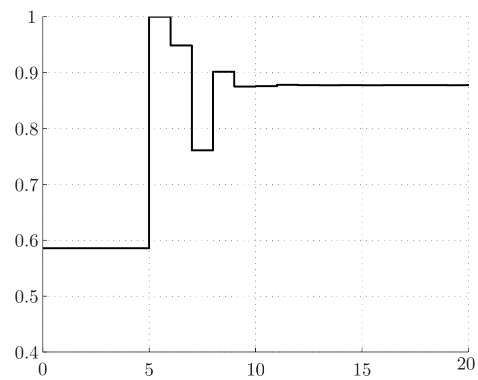


(b) Duty cycle $d(t)$

Fig. 7. Closed-loop simulation of the converter during a step-up change in the input voltage



(a) Output voltage $v_o(t)$



(b) Duty cycle $d(t)$

Fig. 8. Closed-loop simulation of the converter during a step-down change in the input voltage

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