Leakage Current Mitigation in Photovoltaic String Inverter Using Predictive Control With Fixed Average Switching Frequency

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***Abstract*—This work proposes and validates model predictive control as an alternative control strategy for H-NPC converters for single-phase grid-tied string photovoltaic systems. The presented control scheme achieves the good quality current waveforms with unity power factor, dc-link voltage control, neutral-point voltage minimization. Furthermore, the predictive controller has been further enhanced by including an average device switching frequency restriction and a dv/dt mitigation. The main contribution of this paper is the avoidance of the potential leakage current due to parasitic capacitance of the photovoltaic modules by using a predictive model based control technique instead of modulated-schemes and eliminating high-frequency common-mode voltage components. Experimental results during steady state and dynamic operation are presented to illustrate the behavior of the H-NPC converter commanded by the proposed control scheme.**

***Index Terms*—Photovoltaic Applications, Multilevel Converters, Grid-Connected PV Converters, Predictive Control.**

I. Introduction

SINGLE-PHASE grid-tied photovoltaic (PV) systems have become a grown industrial technology with global presence. Several power converters have found commercial acceptance, among them, the H-bridge, H5, HERIC, H6, T-type, and the single-phase three-level Neutral-Point-Clamped (NPC) [1], [2]. The search for more efficient, reliable, grid compliant and proprietary technology differentiation is the main responsible of the outstanding development and diversity of power converter topologies. As of publication of this manuscript, the H-bridge NPC (H-NPC) has been commercialized by ABB under the name of PVS300-TL up to 8kW for small-scale rooftop PV applications. The H-NPC converter consists of the single-phase bridge connection of two three-level NPC converter legs, forming a five-level converter. Although five-level voltage waveform is available, a particulary three-level carrier-based Pulse-Width-Modulation (PWM) scheme has been carry out in [3] in order to avoid switched common-mode voltages (CMV) that could give rise to leakage currents through the PV system parasitic capacitance and grounded metallic frame [4].

Leakage current mitigation can be addressed by several methods according with the established literature. Some of them are shown in Fig. 1. The first method is done by changing the power topology inverter, e.g., the conventional H-bridge inverter is modified by including one or two semiconductors forming the well-known H5 and H6 inverter [5]–[7], respectively. Thus, by using a correct modulation scheme the switched CMV can be constant [8] or with low-frequency components only. The second method is based by including an extra output filter stage to reduce the leakage current as has been reported in [9], [10]. The third method is by modifying the modulation scheme of conventional inverters [11]–[14]. Finally, other option to address the leakage current issue is by changing the control scheme, which gives the break through to this paper.

H-NPC topology is commonly used in rooftop PV systems thanks to the lower voltage requirements at the dc-link respect to conventional NPC topology [2], which reduces the number of PV panels required to achieve a proper operation, providing more flexibility for the system design. In fact, the MPPT voltage range is increased due to the H-bridge connection, while the blocking voltage of each semiconductor is $V_{dc}/2$ instead of rated voltage. This advantage allows the possibility to increase the dc-link voltage value to e.g., 1kV without a dc-dc booster stage. Another advantage is the simplicity of the power circuit, due to all the power valves switch at the same switching frequency, simplifying the thermal dissipation. Finally, in the H-NPC topology the CMV minimization is achieved by modifying the modulation stage as is implemented by the commercial manufacturer, or control stage as is implemented in this paper, without any extra hardware, e.g. filters, ac or dc extra switches, dc-dc converters with HF isolation. From the above reasons, we use the H-NPC as an example case where the converter freedom degree can be used avoid leakage currents.

Nowadays, essentially one control strategy for grid-tied

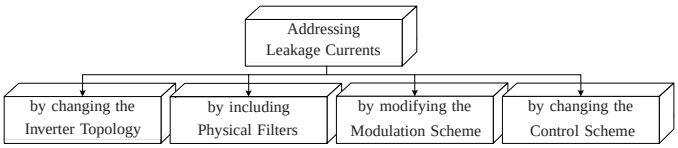

Fig. 1. General classification of leakage currents mitigation methods in transformerless inverters.

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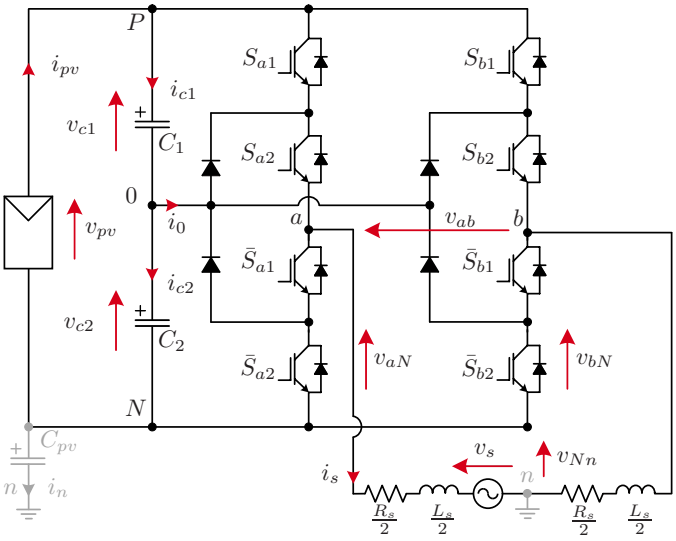

Fig. 2. Topology of a single-phase grid-tied H-NPC PV inverter.

power converters has lead high-performance industrial applications: the voltage-oriented control (VOC) [2]. Conventional and new control schemes are fully programmed on high flexibility digital platforms. Digital Signal Processors (DSPs) enable the integration of more functionality and the implementation of more complex control strategies or variations of conventional schemes, e.g., virtual flux-oriented control (VFOC) [15] or model predictive control (MPC) [16]. Increasing attention has been dedicated to the use of MPC in power electronics applications due to the development of advanced DSPs with continuously decreased cost [1], [17]. In fact, the utilization of MPC in power systems has been proved experimentally by applying Continuous Control Set (CCS) and Finite Control Set (FCS) techniques [16]. The predictive approach is based on the calculation of the future discrete system dynamic to compute optimal actuation variables, allowing a fast dynamic response with flexible control routine and the possibility to include constraints. [18], [19]. Finally, FCS-MPC has been introduced as a promising control algorithm for power converters and drives [18], [20].

The contributions of this paper are three. The first one is the use of a moving-window to compute the average device switching frequency with negligible computational cost, which allows one to control and almost fix the average switching frequency, that usually is a challenge in predictive control. The second one is the minimization of the CMV to avoid potential leakage currents. In addition, a very simple normalization method to select the weighting factors is presented to reduce the converter commissioning. We present a full description of the experimental set-up and results that validates the grid current control with unity power factor, neutral-point voltage (NPV) minimization and non-switched CMV to avoid leakage currents.

II. System description

The schematic of the PV energy conversion system based on the H-NPC is illustrated in Fig. 2. The converter is built with two three-level NPC (3L-NPC) legs connected as an H-Bridge. The H-NPC output is connected to the ac-grid through a symmetrically divided inductive filter L_s where the

TABLE I
Switching state table of the H-NPC PV inverter

State	S_{a1}	S_{a2}	S_{b1}	S_{b2}	v_{ab}	i_0	$v_{aN}+v_{bN}$
0	1	1	1	1	0	0	$2v_{dc}$
1	1	1	0	1	$v_{dc}/2$	$-i_s$	$3v_{dc}/2$
2	1	1	0	0	v_{dc}	0	v_{dc}
3	0	1	0	0	$v_{dc}/2$	i_s	$v_{dc}/2$
4	0	1	0	1	0	0	v_{dc}
5	0	1	1	1	$-v_{dc}/2$	i_s	$3v_{dc}/2$
6	0	0	1	1	$-v_{dc}$	0	v_{dc}
7	0	0	0	1	$-v_{dc}/2$	$-i_s$	$v_{dc}/2$
8	0	0	0	0	0	0	0

resistor R_s is for modeling purposes only. Each NPC branch can generate three voltage levels ($v_{dc}/2$; 0; $-v_{dc}/2$). The H-bridge connection of both legs achieves a five-level output voltage waveform (v_{dc}; $v_{dc}/2$; 0; $-v_{dc}/2$; $-v_{dc}$). The firing signals of each power switch, the output voltage defined as $v_{ab} = v_{aN} - v_{bN}$ and the current out from the neutral-point i_0, in function to each of the nine commutation states, are presented in Table I. Each state S_j, with $j \in \{0, 1, \ldots, 8\}$ defines the firing signals S_{a1}, S_{a2}, S_{b1} and S_{b2} for each switch. Therefore, the output voltage v_{ab} depends on the used j-th state and it can be calculated as

$$v_{aN} = S_{a1}v_{c1} + S_{a2}v_{c2}, \tag{1}$$

$$v_{bN} = S_{b1}v_{c1} + S_{b2}v_{c2}, \tag{2}$$

$$v_{ab} = v_{aN} - v_{bN} = (S_{a1} - S_{b1})v_{c1} + (S_{a2} - S_{b2})v_{c2}, \tag{3}$$

where v_{c1} and v_{c2} are the capacitor voltages and $v_{pv} = v_{dc} = v_{c1} + v_{c2}$ is the overall dc-link potential. The equation that represents the grid current dynamic is,

$$v_{ab} = L_s\frac{di_s}{dt} + R_s i_s + v_s, \tag{4}$$

where R_s and L_s are the mains filter parameters, v_{ab} is the converter output voltage, v_s and i_s are is the mains voltage and current, respectively.

It is well-known that in PV installations appear a parasitic capacitance between their positive and negative terminals respect to the grounded metallic frame of each module [1], [4], as is plotted in gray line in Fig. 2. Thus, the resulting leakage current i_n through the parasitic capacitance is mitigated if the CMV v_{Nn} is constant between two switching intervals. This CMV of the H-NPC converter is depicted in Fig. 2 and can be easily calculated by solving the following system equations

$$v_{Nn} + v_{aN} - \frac{L_s}{2}\frac{di_s}{dt} - \frac{R_s}{2}i_s - v_s = 0, \tag{5}$$

$$v_{Nn} + v_{bN} + \frac{L_s}{2}\frac{di_s}{dt} + \frac{R_s}{2}i_s = 0, \tag{6}$$

with v_{aN} and v_{bN} being the voltages with respect to the negative bus N. Then, by solving (5)-(6), the CMV v_{Nn} can be modeled as the sum of a low frequency voltage component (v_s) and a high frequency voltage part ($v_{aN} + v_{bN}$), i.e.,

$$v_{Nn} = \frac{v_s}{2} - \frac{v_{aN} + v_{bN}}{2}, \tag{7}$$

where the term $v_{aN} + v_{bN}$ depends instantly on each commutation state and it can assume five different values which are presented in Table I. Unlike the NPC converter, the H-NPC can generate five-levels and more redundant switching states as presented in Table I. In fact, with the H-NPC the control algorithm flexibility is improved, allowing the inclusion of control goals with less impact on the output

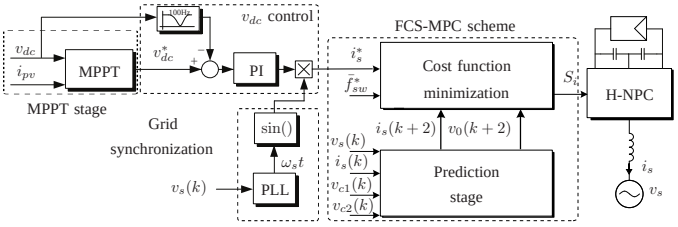

Fig. 3. Proposed control scheme for the H-NPC PV system.

waveform, i.e., capacitor balance through the NPV. This results in an important advantage as it adds more flexibility to the control algorithm, allowing the capacitor balancing through the NPV minimization and other control goals with less impact on the output waveform.

III. Proposed Control Scheme

The implemented control strategy, depicted in Fig. 3, replaces the inner current control loop, the modulation block and capacitor balancing control by a FCS-MPC algorithm. It maintain the Maximum Power Point Tracking (MPPT) algorithm and the outer dc-link voltage control loop that generates the grid current reference. Perturb and Observe (P&O) algorithm is implemented in this validation, mainly due to its simplicity, the low number of measured parameters, its mainstream use and the good experimental results [21]. Therefore the dc-link voltage reference switches in steady state with a three voltage levels fashion. Nevertheless any other MPPT stage could be used, and it does not compromise the verification of the proposed control strategy [21], [22].

A. Dc-Link Voltage Control Loop

The dc-link voltage is controlled with the adjustment of the active power injected to the grid. For this, the error $v_{dc}^* - v_{dc}$ is controlled with a proportional-integral (PI) controller that generates the reference for the delivery grid current. The design procedure can be summarized with a simple parameter adjustment by using a bandwidth of 2Hz with a damping ratio of ξ=0.707, which establishes a compromise between voltage speed tracking and overshoot response. To obtain a correct controller is needed a representation of the dc-link voltage v_{dc} respect to the magnitude of the grid current $\hat{I}_s$. Thus, the following transfer function is used,

$$h_{vdc}(s) = \frac{v_{dc}(s)}{\hat{I}_s(s)} = -\frac{k_{dc}}{\tau_{dc}s + 1}, \tag{8}$$

where k_dc and τ_{dc} has been computed by using the procedure reported in [23]. Furthermore, due to the capacitors charge and discharge, the voltage v_{dc} has a continuous and an oscillatory component at $2f_g$=100Hz. The optimal voltage control is fulfilled with a filtering block prior to the dc-link voltage measurement, through a notch filter tuned to 100Hz as is depicted at the left of Fig. 3. To ensure an unity power factor, Phase-Locked-Loop (PLL) based on a Second-Order Generalized Integrator with Quadrature Signal Generator (SOGI-QSG) is here [24]. As a result, a sinusoidal reference i_s^* for the grid current is imposed.

B. Predictive Current and Neutral-Point Voltage Control

The grid current is regulated through the conventional FCS-MPC strategy. Following this algorithm, the nine valid switching states of the H-NPC converter defined in Table I are used. In order to derive an analytic expression for the current prediction, it is necessary to express the relation between the voltage v_{ab} and the grid current i_s in discrete time, from which the future value of the current can be calculated by using a first order Taylor series,

$$i_s(k+1) = i_s(k)\left(1-\frac{R_sT_s}{L_s}\right) + \frac{T_s}{L_s}\left(v_{ab}(k)-v_s(k)\right), \tag{9}$$

where T_s=32μs is the sampling period. Hence the future value of the grid current can be predicted as a function of the system measurements and the feasible output voltages v_{ab}.

As is illustrated in Table I, it can be seen that the current i_0 going out from the neutral-point varies with respect to the applied switching state. To compute this current, the following definitions related to the capacitor currents are required,

$$i_{c1} = C_1\frac{dv_{c1}}{dt} = i_{pv} - (S_{a1} - S_{b1})i_s, \tag{10}$$

$$i_{c2} = C_2\frac{dv_{c2}}{dt} = i_{pv} - (S_{a2} - S_{b2})i_s, \tag{11}$$

$$i_0 = i_{c1} - i_{c2} = -(S_{a1} - S_{b1} - S_{a2} + S_{b2})i_s, \tag{12}$$

where i_{c1} and i_{c2} are the currents related with each capacitor and illustrated in Fig. 2. Assuming that $C_1 = C_2 = C_{dc}$, the neutral-point potential v_0 depends dynamically on the neutral-point current and it can be obtained as,

$$v_0 = v_{c1} - v_{c2}. \tag{13}$$

$$\frac{dv_0}{dt} = \frac{dv_{c1}}{dt} - \frac{dv_{c2}}{dt}, \tag{14}$$

where v_{c1}, v_{c2} are the capacitor voltages and its derivatives are directly obtained from (10) and (11). Note that, the term $-(S_{a1} - S_{b1} - S_{a2} + S_{b2})i_s$ corresponds exactly to the neutral-point current in (12). Thus, the final relation is stated for the neutral-point voltage dynamic,

$$\frac{dv_0}{dt} = -\frac{1}{C_{dc}}(S_{a1} - S_{b1} - S_{a2} + S_{b2})i_s = \frac{1}{C_{dc}}i_0. \tag{15}$$

Thus, the neutral-point potential prediction is given by,

$$v_0(k+1) = v_0(k) + \frac{T_s}{C_{dc}}i_0(k). \tag{16}$$

Note that, in digital implementations the time required to compute the control actuation takes a considerable portion of the sampling interval T_s, resulting in one sampling delay. Then, to take this computation time delay into account, variables at $(k+1)T_s$ are extrapolations used as an initial condition for prediction variables at $(k+2)T_s$ [18]. We define the overall cost function defined as g with the two terms,

$$g = \lambda_i^2 g_i^2 + \lambda_b^2 g_b^2, \tag{17}$$

$$g_i = \frac{i_s^* - i_s(k+2)}{I_s^{\max}}, \tag{18}$$

$$g_b = \frac{0 - v_0(k+2)}{V_{dc}^{\max}}, \tag{19}$$

where λ_i and λ_b are the weighing factors associated with grid current regulation and neutral-point potential minimization, respectively. Then, the scalar cost function g is computed for

all the feasible actuation and the optimal solution is given by

$$\mathbf{S}[j_{op}] = \arg \min_{j \in \{0,\dots,8\}} g[j]. \quad (20)$$

C. Dv/dt Limitation

In order to reduce the dv/dts, only the existing and adjacent voltage levels are allowed to be selected. This emulates something that would naturally result with carrier-based PWM methods [25]. The switching states are chosen according to the minimization of g. This is why there are some cases where $|v_{ab}(k+1) - v_{ab}(k)| > v_{dc}/2$, e.g., the transition between the state number 2 ($v_{ab}(k+1) = v_{dc}$) and the state number 7 ($v_{ab}(k+1) = -v_{dc}/2$) is a feasible path without actuation restrictions. This produce high voltage changes and therefore, more switching losses in the respective semiconductors.

Feasible voltage level paths for an instant k and the corresponding near levels for the next one $k+1$. Thus, by implementing this voltage restriction it is possible to achieve a dv_{ab}/dt reduction. This available state reduction gives the advantage to decrease of the computation time. This is because now, only between three to seven states are evaluated, in comparison to the fixed nine states of the algorithm without any dv_{ab}/dt limitation. A simple logic is implemented to avoid dv_{ab}/dt during the control operation [26]. This logic is based on the knowledge of the state $\mathbf{S}[j_{op}]$ that is being applied.

D. Average Switching Frequency Control

An important characteristic of FCS-MPC is an inherently wide switching frequency range [16]. This lead to high switching losses per semiconductor, which hinders the system performance. Several methods have been proposed in the literature to address this issue without using modulator. The most basic solution is a straight forward penalization over the commutation [27], which lead to a reduction in the switching frequency but with no control over the resultant value. This strategy is complemented in [28] with a PI controller to dynamically modify the weight associated with the commutation, though this PI is not easy to tune appropriately. Other methods solve the problem by improving output current spectrum, either by favoring a certain commutation frequency [29] or by reducing certain bands [30], [31].

These strategies, though effective, are quite hard to implement and tune, making them less attractive for this work. Thus, a Sliding Window approach is performed, where a reference is set to the number of commutations that occurs in a set time. This approach leads to a very well defined average frequency, while also requiring low computation and programming effort. Based on the problem characteristics, the choice of Sliding Window is selected for the system. On the other hand, in recent reported MPC methods, e.g., Modulated MPC, CCS-MPC and others, a terminal modulation stage have been included to fix the switching frequency. However, the hardware implementation simplicity of the conventional FCS-MPC is lost, due to dedicated PWM hardware is required.

In this work a sliding window algorithm is implemented, in which the average device switching frequency is computed. The predicted average switching frequency is compared to a limit value $\bar{f}^*_{sw}$=2.2kHz. For this, the firing signals used for

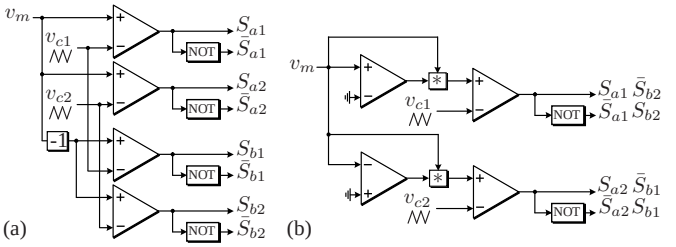

Fig. 4. Modulation schemes for H-NPC PV inverter: (a) conventional LS-PWM and (b) modified LS-PWM by [3].

each device are stored for a fixed time period (good results were obtained with the fundamental grid period $T_1 = 1/f_g$). Since each vector size depends on the sample time T_s, the vectors must store T_1/T_s values. After this procedure, the ON/OFF changes on each vector are added and the results are stored in integer values referred to as nc_{Sxy}. Thus, the average device switching frequency can be approximated by $\bar{f}_{Sxy} = nc_{Sxy}/(2T_1)$. The scalar function (17) is modified by adding the average switching frequency limitation,

$$g_f = \frac{1}{f^{\max}_{sw}} \left(\sum_{x=a}^{b} \sum_{y=1}^{2} W_{Sxy} \left(\bar{f}^*_{sw} - \bar{f}_{Sxy}(k+2) \right)^2 \right)^{\frac{1}{2}}, \quad (21)$$

$$g = \lambda_i^2 g_i^2 + \lambda_b^2 g_b^2 + \lambda_f^2 g_f^2, \quad (22)$$

where λ_f is a constant weighting factor to give importance to this goal respect to the other objectives and W_{Sxy} is time-varying weighting factor for each commutation function. It is important to highlight that the classical way to weight a cost function imposes an average switching frequency as reference $\bar{f}^*_{sw}$. Nevertheless, the desired outcome is the limitation of the commutation with a maximum frequency and the release of the frequency control when the system is below the reference boundaries. This restriction is achieved with a time-varying weighting factor W_{Sxy} defined as follows,

$$W_{Sxy} = \begin{cases} 1 \text{ if } \bar{f}_{Sxy} > \bar{f}^*_{sw} \\ 0 \text{ if } \bar{f}_{Sxy} \leq \bar{f}^*_{sw} \end{cases} \quad \forall\ x \in \{a,b\},\ y \in \{1,2\}. \quad (23)$$

E. Common-Mode Voltage Control

In transformer-less grid-tied PV inverters, the switched CMV respect to the ground produces a dv/dt across these parasitic capacitances between the positive and negative dc bus respect to the grounded frame of the PV array drawing a leakage current i_n. The CMV depends on the inverter topology, the mains filter and the modulation strategy [8], [13]. Fig. 4a illustrates the conventional Level-Shifted PWM (LS-PWM), where the output voltage have five-levels and switched CMV, which produce leakage currents. To avoid this high-frequency components, a modified LS-PWM (mLS-PWM) is adopted in order to generate non-switched CMV, which is depicted in Fig. 4b. The above particular modulation reduces the power quality of the converter since only three-level voltages can be utilized [3]. However, the maximum output voltage level V_{dc} is the retained.

In the proposed control scheme there is no a modulation strategy, thus an additional term is added to the cost function to achieve the same objective. The CMV v_{Nn} respect to the negative bus N on Fig. 2 and computed in (7), where it can be modeled as the sum of a low frequency voltage (v_s) and a high frequency voltage ($v_{aN} + v_{bN}$). This term

TABLE II
ACCEPTABLE ABSOLUTE ERRORS

Variable	Max. Value	ε_{Is}	ε_{V0}	ε_{fsw}	ε_{Vcm}
Max. grid current, $I_s^{\max}$	10A	0.1	-	-	-
Max. dc-link voltage, $V_{dc}^{\max}$	200V	-	0.2	-	-
Max. av. switching Freq. $f_{sw}^{\max}$	2.5kHz	-	-	40	-
Max. common-mode voltage $V_{cm}^{\max}$	400V	-	-	-	8

TABLE III
SYSTEM PARAMETERS

Description	Symbol	(SI)	(pu)
General Parameters			
Rated active power	P_{pv}	1.0kW	1
Grid voltage line-neutral (rms)	V_s	110V	1
Rated dc-link voltage	V_{dc}	190V	1.73
Grid frequency	f_g	50Hz	1
Filter inductance	L_s	3mH	0.12
Filter losses	R_s	0.15Ω	0.018
dc-link capacitance	$C_1 = C_2$	3.9mF	9.88
dc-link resistor losses	$R_{c1} = R_{c2}$	10$k\Omega$	1.24k
PV String Parameters			
Serie and parallel PV modules	n_s, n_p	4, 1	-,-
Max. power of PV-mod.	P_{pm}	125.93	0.084
Open circuit voltage of PV-mod.	V_{oc}	52.30	0.531
Max. power voltage of PV-mod.	V_{pm}	47.70	0.43
Short circuit current of PV-mod.	I_{sc}	2.81	0.21
Max. power current of PV-mod.	I_{pm}	2.64	0.19
Control Parameters			
Av. switching frequency limit	$\bar{f}_{sw}^*$	2.2kHz	40
Sampling time	T_s	32μs	625
dc-link voltage design	BW, ξ	2Hz, 0.707	-,-
dc-link voltage PI Controller	k_p, k_i	-0.0408, -0.177	-,-
P&O updating period	T_{mppt}	2s	100
P&O updating voltage step	ΔV_{mppt}	5V	0.045
Weighting factors	λ_i, λ_b	0.1k, 1k	-,-
Weighting factors	λ_f, λ_n	62.5, 50	-,-

depends directly on each switching state and has a variable waveform of five different values as summarized in Table I and only the states 2, 4 and 6 can be selected to achieve the v_{Nn} minimization, while the output levels are reduced to only three different values, v_{dc}, 0 and $-v_{dc}$. Thus, the resulting leakage current i_n is mitigated if the CMV is fixed due to $i_n \approx C_{pv} dv_{Nn}/dt$, where C_{pv} is the equivalent parasitic capacitance of PV modules respect to the grounded frame. This control goal can be allowed by the new cost function

$$g_n = \frac{v_{dc} - (v_{aN} + v_{bN})}{V_{cm}^{\max}}, \tag{24}$$

$$g = \lambda_i^2 g_i^2 + \lambda_b^2 g_b^2 + \lambda_f^2 g_f^2 + \lambda_n^2 g_n^2, \tag{25}$$

where λ_n is a constant scalar factor that enables the CMV control. Finally, a normalization method to select the weighting factors used in experimental results is presented.

F. Weighting Factor Adjustment

In the literature there are two ways to select the weighting factors associated with each control objective. The first one uses iterative offline simulations to achieve a desired outcome, and the second one expresses some mathematical dependencies between the control goals [16]. A different procedure, in the line of the second method, is explored to select these scalar factors. The goal in this procedure is to weigh each of the different errors such that the value generated in the cost function is comparable in magnitude between each other, thus making all objectives relevant to the cost function. This can be achieved by making an estimation on the average absolute error, ε_i expected for each i-th variable presented in Table II.

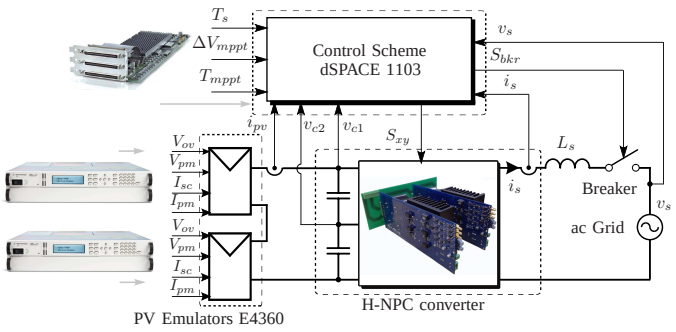

Fig. 5. Simplified diagram of the experimental set-up.

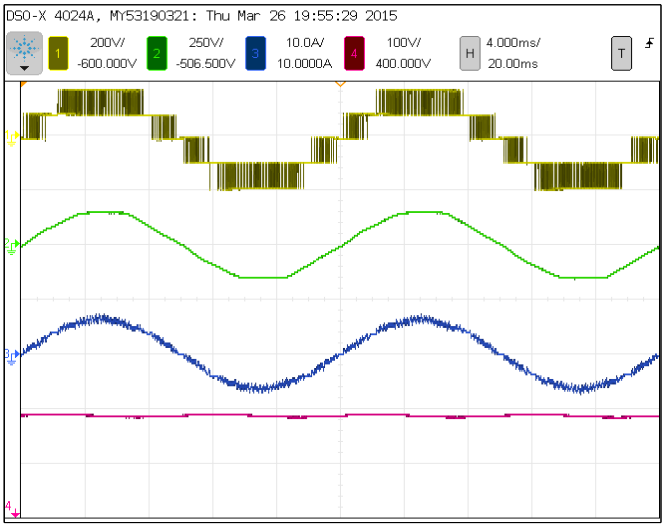

Fig. 6. Experimental results in steady state: CH1) inverter voltage (yellow), CH2) grid voltage (green), CH3) grid current (blue) and CH4) dc-link voltage (red).

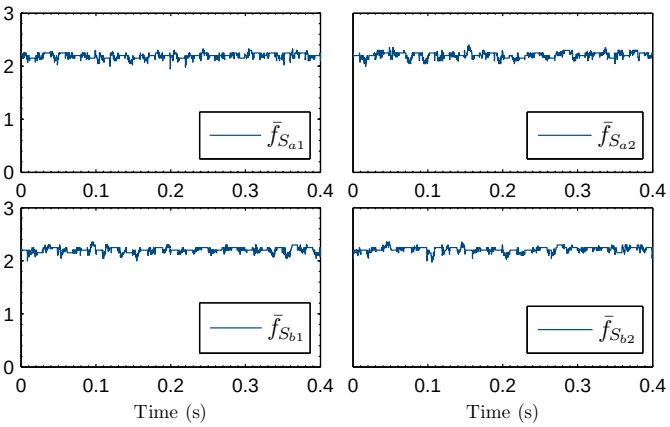

Fig. 7. Experimental results of average device switching frequency in kHz.

This allows to weigh each error such that all the cost function elements give the same value. Then, the weight values α, β, γ and δ are chosen to fit this goal as follows,

$$\alpha = \frac{\varepsilon_{Is}}{Is^{max}} = .01, \tag{26}$$

$$\beta = \frac{\varepsilon_{V0}}{V_{dc}^{max}} = 0.001, \tag{27}$$

$$\gamma = \frac{\varepsilon_{fsw}}{f_{sw}^{max}} = .016, \tag{28}$$

$$\delta = \frac{\varepsilon_{Vcm}}{V_{cm}^{max}} = .02. \tag{29}$$

For the studied system, it is expected to have an average normalized error for each variable as shown in (26)-(29). Finally, each normalized error is weighed by the respective value, such that when a variable reaches the expected error, the respective cost function element shows a value of 1.

$$\lambda_i = \frac{1}{\alpha} = 100, \tag{30}$$

$$\lambda_b = \frac{1}{\beta} = 1000, \tag{31}$$

$$\lambda_f = \frac{1}{\gamma} = 62.5, \tag{32}$$

$$\lambda_n = \frac{1}{\delta} = 50. \tag{33}$$

IV. Experimental Results

A. Set-up Description

The proposed control scheme in Fig. 3 is tested experimentally on an downsized prototype set-up, composed by two NPC legs. Each NPC leg is considered as a Power Electronics Building Block (PEBB) based on the Semikron device SK20MLI066 [32]. The converter is connected to two series PV emulators Agilent E4360 with two channels. Thus, it is obtained a PV string composed by four emulated PV modules. The ac-grid is connected with a circuit breaker and with a reduced voltage value, rated at 110V. The used control, ac-side and dc-side system parameters are fully listed in Table III. The simplified diagram of the experimental setup is depicted in Fig. 5. The algorithm is programmed with C code in a dSPACE 1103 running at $T_s = 32\mu$s.

B. Steady-State Operation

The following experimental results are obtained at emulated Standard Test Conditions (STC) conditions. Note that, the V_{oc} value is slightly higher respect to commercial PV modules due to the fact that the series connection of PV emulators is limited to 240V only.

The performance of the prototype is presented with steady state and dynamic conditions. The first results shows the steady state of the fundamental control variables considering the grid current control, the NPV minimization and the dv/dt and $\bar{f}^*_{sw}$=2.2kHz as is depicted in Fig. 6. Note that, this reference is lower than the conventional switching frequencies (i.e., 5kHz to 20kHz) used in commercial inverters for a grid frequency of 50/60Hz, however the voltage pattern obtained with the proposed control scheme is the same that mLS-PWM proposed in [3] without any modulation scheme.

The five-level stepped voltage waveform of Fig. 6 has been acquired with the digital oscilloscope Agilent DSO-X 4024A and presented in Channel 1 (yellow). Waveforms of Channel 2 (green) and Channel 3 (blue) are the grid voltage and the resultant sinusoidal grid current, which are in phase as a requirement imposed by the user. The flat waveform shape of the grid voltage is due to the polluted grid condition at that time which contains an important component of 5$^{\text{th}}$ and 7$^{\text{th}}$ harmonics. Channel 4 (red) shows the total dc-link voltage. The oscillations of the dc-link voltage represents the well-known 100Hz component due to capacitor charge and discharge and its rms value is 2.55V. The maximum NPV value is 3.09V, while the average voltage is 0.68V.

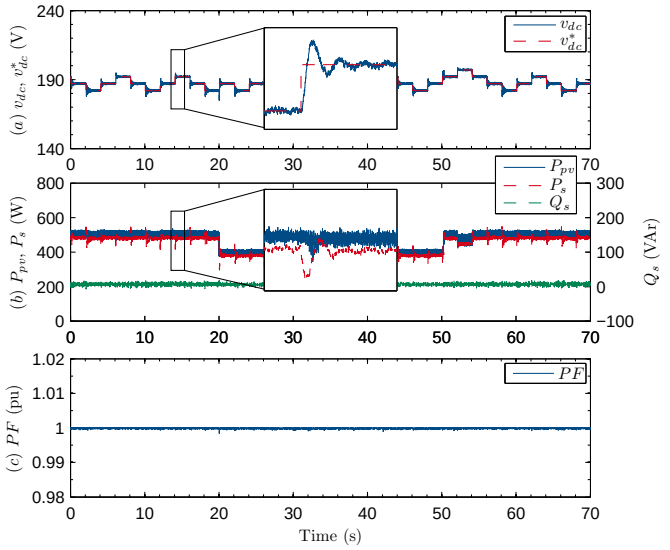

Fig. 8. Experimental results emulating an irradiance change: a) dc-link voltage tracking and its reference, b) total generated PV power, active and reactive power injected to the grid and c) power factor.

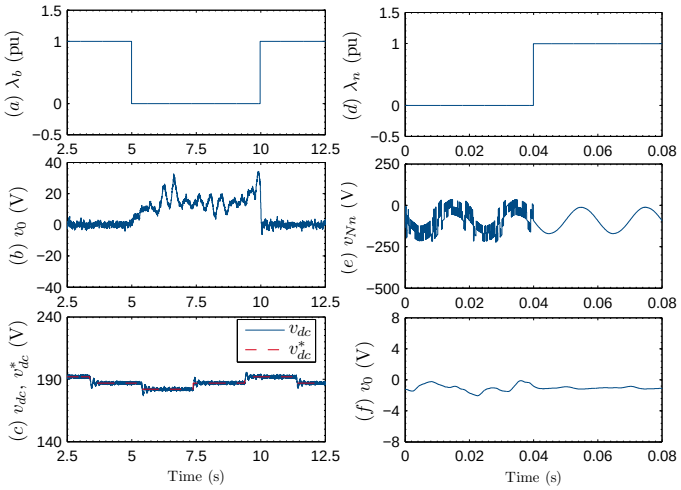

Fig. 9. Experimental results during dc-link capacitor voltages dynamic condition (left) and by enabling CMV control method (right).

The next steady state waveforms are the computed average device switching frequency observed in Fig. 7, where the average switching frequency of each gate signal of the converter are shown. The average value obtained for each gate function is around 2.2kHz with an almost fixed value respect to the fixed imposed constraint f^*_{sw}.

Two general dynamic conditions are experimentally tested. The first one is related to environmental variations, while the second one is related to changes into the control scheme, for example enabling or disabling some weighting factors of the predictive control scheme.

C. Operation during Transients

Firstly, the solar irradiance is decreased from 1.0kW/m^2 to 0.8kW/m^2 at $t = 20$s and then increased back to 1.0kW/m^2 at $t = 50$s. Note that, the P&O MPPT algorithm is applied every 2s with a step voltage of 5V, i.e., a speed range of $V_{track} = 1.25\%$/s [33]. These changes are performed on each

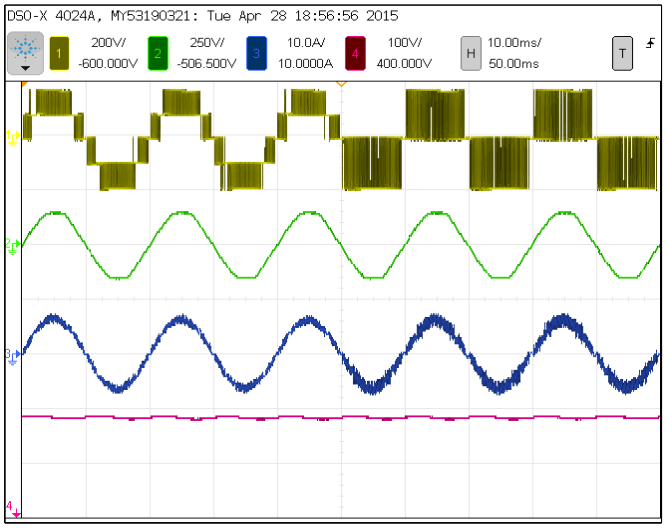

Fig. 10. Experimental results during dynamic conditions with the enable CMV reduction method: CH1) inverter voltage (yellow), CH2) grid voltage (green), CH3) grid current (blue) and CH4) dc-link voltage (red).

PV emulator changing the parameter I_{pm} from 2.64A to 2.04A of the programmed I-V curve for each channel.

As expected, the oscillations of the dc-link voltage represents the waveform obtained with a P&O MPPT method and its value is 2*ΔV_{mppt}=10V. Then, under an irradiance step this well-known fashion is modified as is appreciated at $t = 20$s and $t = 50$s in Fig. 8a. Nonetheless, the mean value voltage reference is retained. Note that, these irradiance steps are not very realistic, but it is considered here to show the effect of an irradiance change on the photovoltaic power system P_{pv} and then over the injected active power P_s as is presented in left scale of Fig. 8b. The reactive power in right scale of Fig. 8b has been imposed to be zero under all the operation time achieving an unity power factor as depicted in Fig. 8c. A zoom of the dc-link voltage with its reference and the powers under an increase MPPT step voltage are included in Fig. 8a and Fig. 8b, respectively.

D. Control Scheme Changes

Two different dynamic tests of the control scheme are experimentally reported. The first one is the disabling of the NPV minimization component on the overall cost function Fig. 9 (left). In Fig. 9a the associated normalized weighting factor is disabled in $t = 5$s and then enabled again in $t = 10$s, resulting a capacitor voltage evolution as presented in Fig. 9b. Note, that the total dc-link voltage tracking (Fig. 9c) remains unchanged under the test.

The second test is related to CMV mitigation Fig. 9 (right). The weighting factor that commands this control objective is enabled in $t = 0.04s$ as shown in Fig. 9d, resulting in a change of the CMV v_{Nn} fashion from high frequency to low frequency waveform at f_g (grid frequency) as is plotted in Fig. 9e, while the NPV minimization is retained as is presented in Fig. 9d. Finally, in Fig. 10, the converter output voltage changes from five to three voltage levels as is illustrated in Channel 1 (yellow). As observed in the previous subsection, with a lower number of voltage levels the resulting low frequencies of the grid current are increased. This issue is depicted in Channel 3 (green).

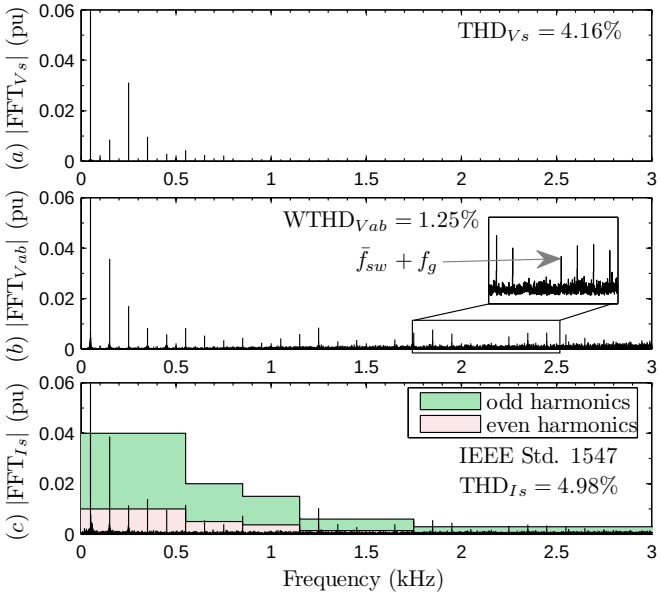

Fig. 11. Experimental spectra with CMV control: FFT of (a) v_s, (b) v_{ab} and (c) i_s.

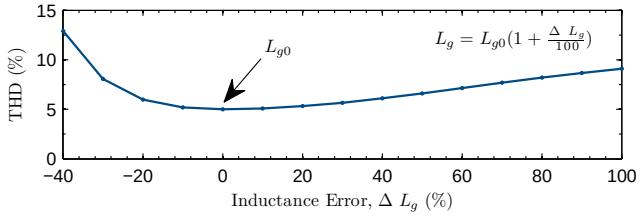

Fig. 12. Experimental THD of grid current by using different inductance errors.

TABLE IV
ALGORITHM EXECUTION TIMES WITH $T_s = 32$ (μs).

Without dv/dt limitation				With dv/dt limitation			
Time	$\bar{x}_t$ (μs)	σ_t (μs)	t_{max} (μs)	Time	$\bar{x}_t$ (μs)	σ_t (μs)	t_{max} (μs)
t_{med}	8.59	0.018	8.67	t_{med}	8.59	0.016	8.67
t_{pll}	4.13	0.084	4.23	t_{pll}	4.15	0.070	4.23
t_{ext}	0.052	0.014	0.054	t_{ext}	0.053	0.013	0.054
t_{mpc}	13.57	0.026	13.65	t_{mpc}	5.29	0.021	5.34
Total	26.88	0.088	27.09	Total	18.57	0.085	18.72

The harmonic response with CMV control is depicted in Fig. 11, where the spectra of v_s, v_{ab} and i_s are presented. The data has been sampled at 31.25kHz, while the FFT analysis has been computed by considering 60 periods of f_g. The harmonic content is plotted until the 60th harmonic (3kHz), with the band-side $\bar{f}_{sw} + f_g$ of the obtained average switching frequency is included in the zoom of Fig. 11b. The resulting grid current THD obtained without and with the CMV minimization is 2.45% and 4.98%, respectively. This THD increment is due to the number of levels of converter output voltage is reduced from five to three levels only allowing the common-mode minimization. In both cases the THD value is below the established by IEEE Std. 1547 [34]. Finally, the CMV minimization is achieved by modifying the modulation stage or control stage only, without any extra hardware. On the other hand, the big cost to perform this modification is an increased THD as has been verified by experimental results, which must be taken into consideration during the design of the inverter filter.

TABLE V
COMPUTATIONAL BURDEN OF PREDICTIVE CONTROL LOOP.

Task	Operations	Without CMV min. (n=9)	With CMV min.(n=3)
Extrapolation	Sums: 11 Products: 7	18	18
Prediction	Sums: $66n$ Products: $47n$	1017	339
Optimization	Sums: $6n$ Products: $6n$	108	36
Total	Sums: $72n$+11 Products: $53n$+7	1143	393

Finally, a sensitivity analysis respect to the normalized inductance error computed as $\Delta L_g = 100\frac{L_g - L_{g0}}{L_{g0}}$ is presented in Fig. 12. Here the nominal value is L_{g0}=3mH, which is the used value in previous experiments. Note that, a positive inductance error has less impact in the resultant THD of grid current than a negative inductance error.

E. Computational Burden Discussion

A computational burden analysis is presented in this section. As expected, implementing the dv_{ab}/dt voltage restriction it is possible to decrease the burden time, due to only three to seven states are evaluated, in comparison to the total nine states of the algorithm without any dv_{ab}/dt limitation. This point is validated including a simple comparison in terms of processing time for both cases. Table IV shows the processing time of each stage considering 2000 iterations, where the time needed for measurements is t_m, the time required for SOGI-QSG PLL and filters is t_{pll}, the time needed for the external control loop is t_{PI} and the time used for the inner control loop (FCS-MPC algorithm) is t_{mpc}. The total average processing times used in the algorithm without and with the dv_{ab}/dt limitation are 26.88μs and 18.57μs, respectively. Thus, with this dv_{ab}/dt limitation a 30% of reduction in the burden time is achieved. Finally, from Table IV, the standard deviation of the calculation time is similar in both cases, while the maximum processing time in both cases is computed to identify the minimum sampling rate needed for the proposed control scheme.

Generally, in FCS-MPC, processing operations are quickly increased if more number of voltage vectors and objectives are used. For this reason, the number of calculations realized by the predictive algorithm is introduced in Table V, while the well-known external lineal controller is omitted. The computation is performed in terms of fundamental operations, such as number of sums and products evaluations. The algorithm has been evaluated by considering (25) without and with CMV voltage minimization, where the number of evaluated voltage vectors varies from 9 to 3. The worst case is obtained for $n = 9$ with a total of 1143 operations, which must be computed in one sampling time. Finally, according with execution times and operations the minimum hardware implementation requirement is a DSP running at 30μs, which is a minor requirement respect to the conventional DSPs used for power applications in the market, e.g., TMS320F28335 or TMS320F28377D.

F. Brief Efficiency and CMV Comparison

A brief comparison in terms of efficiency and CMV of conventional schemes respect the proposed scheme is

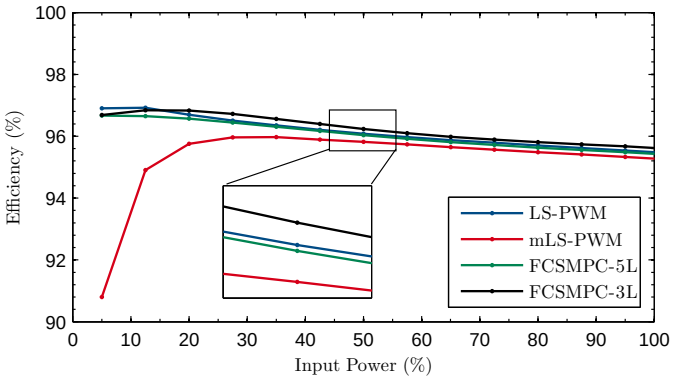

Fig. 13. Efficiency of PR with LS-PWM and FCS-MPC controllers operating at V_{dc}=190V and P_pv=0.1 to 1kW.

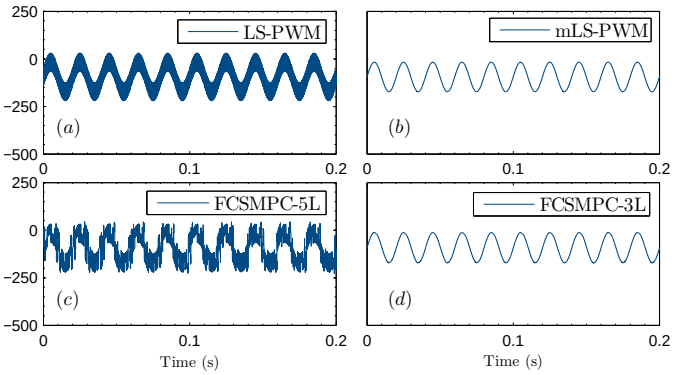

Fig. 14. CMV with a) LS-PWM, b) PR with modified LS-PWM, c) FCS-MPC with five output voltage levels and d) proposed FCS-MPC with three output levels.

presented in this last section. Since the studied power topology is a single-phase system, synchronized reference frame transformations are not directly proper for the grid current control, and therefore resonant controllers (PR) tuned to the grid frequency are required to compare the performance. The design of these controllers is a bit more challenging, as they are more sensitive to mains frequency changes [35].

A relevant merit figure for power converter design applied to PV applications is the converter efficiency respect to the power range. Conduction and switching losses of power switches and resistive losses of passive components are evaluated in this last section, where IGBT power losses are composed by conduction, turn-on and turn-off losses, while the inverse and freewheeling diode power losses are composed by conduction and reverse recovery losses. The conduction losses are obtained directly from the datasheet of the IGBT module [32], while the switching losses model is derived from [36].

In order to quantify the performance achieved with the proposed control scheme respect to conventional ones, the converter efficiency respect to the input power is measured. Fig. 13 illustrates the efficiency results of the system from 5% to full power range by using the parameters summarized in Table III. This figure shows the obtained efficiency for linear PR controller with traditional LS-PWM and commercial mLS-PWM. Furthermore, efficiencies of FCS-MPC operating at natural five output voltage levels and with the proposed high-frequency CMV elimination are included. It is well-known that a reduced overall commutations

number will reduce the switching losses and the efficiency is increased. Thus, a 0.5% of efficiency improvement is achieved with the proposed strategy respect to the solution reported in [3]. Finally, Fig. 14 shows the obtained CMV of the evaluated methods. In conclusion, conventional PR controller with LS-PWM and FCS-MPC with five output voltage levels generate potential leakage currents due to the high-frequency in the resultant CMV, while the solution with mLS-PWM and the proposed FCS-MPC generate only a fundamental low-frequency component.

V. Conclusions

This paper shows the implementation of FCS-MPC on a single-phase photovoltaic grid-connected system based on the commercial H-NPC PV inverter. The programmed control scheme provides current reference tracking, dc-link capacitor voltage balance through the neutral-point voltage minimization and average semiconductor switching frequency limitation. Furthermore, a common-mode voltage minimization has been reported as an attractive method to avoid the potential leakage currents. The proposed control scheme has been satisfactorily validated for steady state and dynamic operation under experimental conditions in a downscaled power converter. Finally, FCS-MPC appears as a very flexible control scheme to grid-tied PV applications.

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