

Model Predictive Direct Current Control of Modular Multilevel Converters: Modelling, Analysis and Experimental Evaluation

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Abstract—Modular multilevel converters (M2LCs) are typically controlled by a hierarchical control scheme, which essentially requires at least two control loops: one to control the load current and another to control circulating currents. This paper presents an M2LC with a single controller, which is based on model predictive direct current control (MPDCC) with long prediction horizons. The proposed MPDCC scheme maintains the load current within tight bounds around sinusoidal references and minimizes capacitor voltage variations and circulating currents. An internal prediction model of the M2LC is used to minimize the number of switching transitions for a given current ripple at steady-state while providing a fast current response during transient conditions. A state-space model, which is generalized for an N number of modules per each arm of the M2LC, is also presented to investigate the dynamic behaviour of arm currents and capacitor voltages. Simulated performance of the converter, under various operating conditions, is presented in comparison to measured performance of a single-phase, three-level 860-VA M2LC prototype to demonstrate the proposed MPDCC philosophy.

Index Terms—Circulating currents, modular multilevel converter (M2LC), model predictive control (MPC), voltage balancing.

I. INTRODUCTION

Modular multilevel converter (M2LC) topology has recently become popular in medium to high voltage applications [1]–[3]. M2LC exhibits modularity, scalability, reduced voltage rating of the switches and redundant switching operations. A number of advantages associated with these features make M2LC suitable for various applications, such as high-voltage direct current (HVDC) transmission [4], motor drives [5], traction motors [6] and static synchronous compensator (STATCOM) [7].

In general, load currents of M2LC are controlled taking into account capacitor voltages and circulating currents so as to ensure stable operation of the converter. The importance of balancing capacitor voltages around their nominal values has been acknowledged in [8]–[13]. Circulating currents or balancing currents are inherent to the M2LC topology and manifest from variations in the capacitor voltages in combination with the modulation scheme [3], [14]. If these currents are not controlled or minimized, then the arm currents, rating of

the switches and conduction losses will all increase. Various control schemes, mostly cascaded, have been proposed to minimize these features [5], [13], [15], [16]. These schemes employ two control loops, where an upper loop uses a current controller in conjunction with a modulator to control the load currents. A lower loop utilizes the redundancy of the converter switching states to balance the capacitor voltages. In addition, circulating currents are minimized by adding an appropriate signal to the modulating signal of either each arm or module of the M2LC.

M2LC, being a multi-input multi-output (MIMO) system, has been controlled with schemes that were designed for single-input single-output (SISO) systems. One such commonly used scheme is proportional plus integral (PI) control in combination with a carrier-based pulse width modulation (PWM). Multiple PI loops, which are commonly used to control M2LC, are difficult to tune and could affect the performance of the converter. Model predictive control (MPC) is suitable for controlling MIMO systems in a comprehensive manner [17]. Some of the advantages of the MPC are simple design, ease of handling constraints, ease of modelling various time delays and robustness. MPC has widely been used in the process industry and has recently become popular in power electronics applications [18]–[21].

Because of a number of advantages of MPC over traditional control schemes, it is becoming popular for controlling the M2LC [22]–[25]. These MPC schemes have a single control loop to control the load currents, where error between the references and the predicted load currents is minimized. Variations in the capacitor voltages, circulating currents and the error are all part of a cost function that is evaluated for all the switch positions. The switch position with the minimum cost is applied to the converter and a receding horizon policy is implemented by evaluating the cost function at each sampling instant.

This paper presents a model predictive direct current control (MPDCC) scheme with long prediction horizons to control a M2LC [2], where the controller directly sets the M2LC switch positions without a modulator [21]. MPDCC uses a single control loop to control the load currents within the allocated bounds and to minimize capacitor voltage variations and circulating currents. Moreover, the bounds of the load currents set the level of total harmonic distortion (THD) of the currents and, over a certain range, the THD is a linear function of the bound width. MPDCC differs from the above

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mentioned MPC schemes in a number of ways:

- 1) MPDCC does not minimize the error between the references and predicted load currents, but the error is always kept within the allocated bounds.
- 2) Previously mentioned MPC schemes have a prediction horizon of one, whereas MPDCC yields prediction horizons that are significantly longer than one.
- 3) Unlike the MPC schemes, MPDCC scheme formulates a cost function that accounts for the number of switching transitions or switching frequency and evaluates the cost function over a long prediction horizon.

This paper also presents a generalized state-space model characterizing the dynamics of the M2LC and the model is used for predictions of various variables. Viability of the proposed MPDCC scheme is verified using PLECS/Simulink simulations and experiments for a single-phase three-level 860-VA M2LC prototype. Both simulated and experimental results are in good agreement and demonstrate the benefits of the proposed MPDCC scheme.

II. GENERALIZED MATHEMATICAL MODEL

A typical M2LC is shown in Fig. 1, where each phase-leg of the converter is divided into two halves, called arms. Each arm consists of N modules, which are represented as M_{rn} , $r \in \{a, b, c\}$, $n \in \{1, 2, \dots, 2N\}$, a resistor, R , that models conduction losses and an arm inductor, L . A typical module is configured as a half-bridge converter with a capacitor, C , connected to its terminals. The individual module has two switching states $u_{rn} \in \{0, 1\}$, where 1 means that the capacitor is connected to the circuit, i.e. switch $S_{rn,1}$ is turned on. Mostly, the M2LC is driven such that there are N modules connected in series across the dc-link and the capacitor voltages, $V_{c,rn}$, are balanced around their nominal value, which results in at least $2N + 1$ line-line voltage levels.

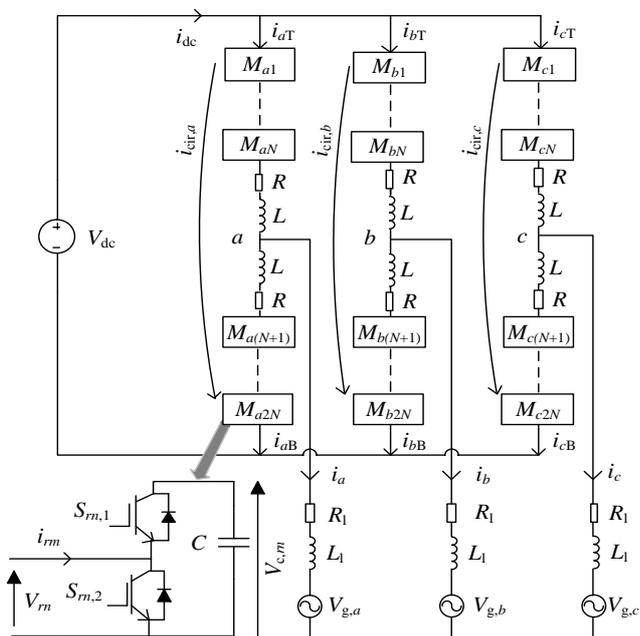


Fig. 1: A typical modular multilevel converter and a module.

Further details on the operating principle and characteristics of the M2LC can be found in [1]–[3].

State of the arm currents and capacitor voltages is modelled using two linear state-space equations, termed as the first and second model, respectively. State variables of the first model are the arm currents in phases a and b , dc-link current and grid voltages in the alpha/beta, $\alpha\beta$, coordinate system. The state vector of the model is defined as

$$\mathbf{x}_i = [i_{aT} \ i_{aB} \ i_{bT} \ i_{bB} \ i_{dc} \ V_{g,\alpha} \ V_{g,\beta}]^T \quad (1)$$

and the input vector is formed by the switching states of the modules

$$\mathbf{u} = [u_{a1} \ u_{a2} \ u_{a3} \ \dots \ u_{c2N}]^T \in \{0, 1\}^{6N} \quad (2)$$

The continuous-time state equation of the first model can be defined as

$$\mathbf{T} \frac{d\mathbf{x}_i}{dt} = \mathbf{F}_i \mathbf{x}_i + \mathbf{G}_i \mathbf{u} + \mathbf{V}_{dc} \quad (3)$$

The definitions of the system matrices \mathbf{T} , \mathbf{F}_i , \mathbf{G}_i and \mathbf{V}_{dc} can be found in Appendix A.

State variables of the second model are the capacitor voltages, and its state vector is defined as

$$\mathbf{x}_c = [V_{c,a1} \ V_{c,a2} \ V_{c,a3} \ \dots \ V_{c,c2N}]^T \quad (4)$$

With the input vector defined in (2), the continuous-time state equation of the model can be defined as

$$\frac{d\mathbf{x}_c}{dt} = \mathbf{F}_c \mathbf{x}_c + \mathbf{G}_c \mathbf{u} \quad (5)$$

The system matrices \mathbf{F}_c and \mathbf{G}_c are defined in Appendix B.

The output equations of the load currents, which are related to the arm currents, i_{rm} , $m \in \{T, B\}$, in phases a , b and c are as follows:

$$i_r = i_{rT} - i_{rB} \quad (6)$$

The equations which define the circulating currents in phases a , b and c are as follows:

$$i_{cir,r} = \frac{i_{rT}}{2} + \frac{i_{rB}}{2} - \frac{i_{dc}}{3} \quad (7)$$

The circulating currents are generated by the voltage difference between the dc-link and the voltage summation of the capacitors that are connected to the circuit [3], [14]. This interdependence between the capacitor voltages and arm currents, where the latter is related to the circulating currents by (7), is further explained with the help of the following equation:

$$R(i_{rT} + i_{rB}) + L \left(\frac{di_{rT}}{dt} + \frac{di_{rB}}{dt} \right) = V_{dc} - \sum_{n=1}^{2N} V_{c,rn} u_{rn} \quad (8)$$

III. PROPOSED CONTROL PHILOSOPHY

Model predictive direct current control (MPDCC), which has its roots in constrained optimal control, has been introduced for multilevel converters [21] and recently for M2LC [2]. In the MPDCC scheme, the output variables are predicted over a number of time steps referred to as the prediction horizon, N_p . The output variables are predicted by considering a number of switching transitions over the length of N_p and the length is referred to as switching horizon, N_s .

A. Control Problem

One of the primary objectives of MPDCC is to keep the load currents within symmetrical bounds around their sinusoidal references. Load currents can be kept within the allocated bounds as long as the value of the violation function, ν_r , with an applied switch position, is zero over the length of prediction horizon, N_p .

$$\nu_r(k) = |i_r(k) - i_{\text{ref},r}(k) - \delta_u| + |i_r(k) - i_{\text{ref},r}(k) + \delta_l| - (\delta_l + \delta_u) \quad (9)$$

Here, $\delta_u = \delta_l = \delta$ is one half of the allowed ripple around the reference current, $i_{\text{ref},r}$.

An inherent characteristic of the M2LC topology is that the capacitors share a part of the dc-link voltage. In general, a control scheme has to balance the capacitor voltages around their nominal value, $V_{c,\text{nom}}$, or minimize the voltage variations, $v_{c,\text{var}}$, around the nominal value.

$$\mathbf{v}_{c,\text{var}}(k) = \begin{bmatrix} V_{c,a1}(k) - V_{c,\text{nom}} \\ V_{c,a2}(k) - V_{c,\text{nom}} \\ \dots \\ V_{c,c2N}(k) - V_{c,\text{nom}} \end{bmatrix} \quad (10)$$

Variations in the capacitor voltages generate circulating currents, as explained in section II, and need to be minimized for the reasons mentioned in previous sections. Therefore, the MPDCC has to determine a switch position that minimizes circulating currents while meeting all other objectives.

$$\mathbf{i}_{\text{cir}}(k) = \begin{bmatrix} i_{\text{cir},a}(k) \\ i_{\text{cir},b}(k) \\ i_{\text{cir},c}(k) \end{bmatrix} \quad (11)$$

At the same time, an average switching frequency, which is an indirect measure of the switching losses, needs to be minimized as well.

B. Prediction Model

Since MPDCC is based on the model of the M2LC, two prediction models of the converter are derived to predict the trajectories of arm currents and capacitor voltages. The first model predicts the arm currents and, as a result, the load currents and circulating currents. The output vector of this model is

$$\mathbf{y}_i = [i_a \ i_b \ i_c \ i_{\text{cir},a} \ i_{\text{cir},b} \ i_{\text{cir},c}]^T. \quad (12)$$

The second model is derived to predict the evolution of the capacitor voltages for the switching states presented in (2). The capacitor voltages are both the state and output vector of this model, $\mathbf{x}_c = \mathbf{y}_c$. Using the continuous-time state equations (1)–(7) and the exact discretization, the following discrete-time models can be derived.

$$\mathbf{x}_i(k+1) = \mathbf{A}_i \mathbf{x}_i(k) + \mathbf{B}_i \mathbf{u}(k) + \mathbf{V}_i \quad (13)$$

$$\mathbf{y}_i(k+1) = \mathbf{C}_i \mathbf{x}_i(k+1) \quad (14)$$

$$\mathbf{x}_c(k+1) = \mathbf{A}_c \mathbf{x}_c(k) + \mathbf{B}_c \mathbf{u}(k) \quad (15)$$

$$\mathbf{y}_c(k+1) = \mathbf{C}_c \mathbf{x}_c(k+1) \quad (16)$$

The definitions of the system matrices \mathbf{A}_i , \mathbf{B}_i , \mathbf{V}_i , \mathbf{C}_i , \mathbf{A}_c , \mathbf{B}_c and \mathbf{C}_c can be found in Appendix C.

C. Control Algorithm

The Switch and Extrapolate (SE) switching scheme is adopted, as described in [2], [21], [26], with N_s of 1 to predict the states of the M2LC. In this scheme, an extrapolation of the predicted load current trajectories yields a prediction horizon, N_p , which is significantly longer than one. The operation principle of the SE scheme is explained below:

- 1) Given the previously applied switch position $\mathbf{u}(k-1)$ and the present states, the arm currents and, as a result, the load currents are predicted at time-step $k+1$ using (13) and (14) for all the switch positions. This implements the first part, S, of the SE scheme. For example, the predicted trajectories of the load currents, in phases a and b , for three switch positions are shown in Fig. 2. Here, δ is one half of the allowed ripple around the reference currents.
- 2) During steady-state operating conditions, the value of the violation function (9) can be kept at zero by imposing constraint on the switch positions. These positions are referred to as the candidate positions. However, during transient operating conditions, such as sudden change of reference currents, current trajectories violate the bounds because of a limited response time of the physical system. Therefore, positions for which the absolute violation value, ν_r , decreases with time are also the candidate positions.

In the next step, candidate switch positions with indices j , where $j \in \mathcal{J}$ and \mathcal{J} is an index set, are determined. Moreover, switch positions for which a load current violates bounds at $k+1$ are rejected. For example, consider Fig. 2, in which the switch position 1 is not a candidate position because the load current is predicted to violate the upper bound, for both phases a and b , at time-step $k+1$. On the other hand, the load current at $k+1$ is predicted to be within the hysteresis bounds when selecting the third switch position, making it a candidate position. For the second position, the current at $k+1$ will remain outside of its bound for phase a , but its violation decreases from k to $k+1$, making it

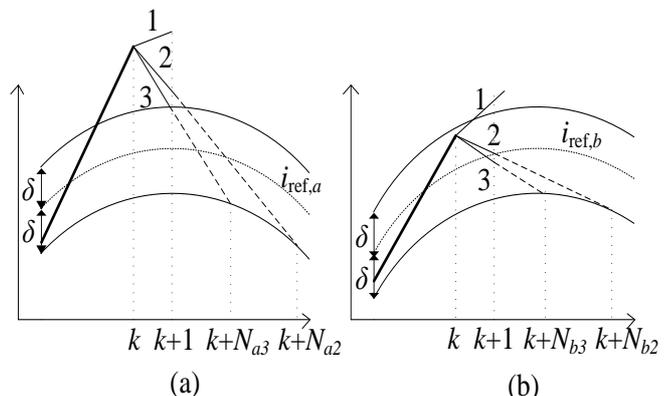


Fig. 2: Trajectories of the load currents (a) phase a and (b) phase b . Actual, predicted and extrapolated trajectories are shown as thick-solid, solid and dashed lines, respectively.

also a candidate position.

- 3) The candidate trajectories are then linearly extrapolated from time-step $k + 1$ onwards until they violate the predefined band [27]. This implements the second part, E, of the SE scheme. This extrapolated length, N_j , is represented in multiples of the sampling interval, T_s . For position 2 at time-step k , the load current trajectories can be kept within the bounds for a length of $N_2 = \min(N_{a2}, N_{b2}, N_{c2})$, before requiring a new switching transition at time-step $k + N_2$.
- 4) At the next stage, predict the capacitor voltages, using (15) and (16), for all the predetermined candidate positions (item 2). These voltages are then linearly extrapolated for the number of time steps determined in item 3. The capacitor voltages at time-step $k + N_j$, $j \in \mathcal{J}$ are denoted as terminal capacitor voltages, $V_{c,rm}(k + N_j)$. Similarly, predict and extrapolate the trajectories of the circulating currents, using (14), for all the candidate positions.
- 5) The candidate positions satisfy the constraint imposed on the load currents and the remaining objectives of the M2LC, as stated in section III-A, are met by evaluating the following cost function for the candidate positions.

$$C_j = \frac{\|\mathbf{u}_j(k) - \mathbf{u}(k-1)\|}{N_j} + \lambda_1 \|\mathbf{v}_{c,var}(k + N_j)\|_2^2 + \lambda_2 \|\mathbf{i}_{cir}(k + N_j)\|_2^2, \quad j \in \mathcal{J} \quad (17)$$

Here, λ_1 and λ_2 are weighting coefficients. The first term in the cost function penalizes the number of switching transitions discounted over the prediction horizon, allowing one to minimize the average switching frequency, and is evaluated by dividing the number of switching transitions by the length of the extrapolated trajectory. The other two terms, as described in section III-A, are used to minimize the voltage variations and the circulating currents.

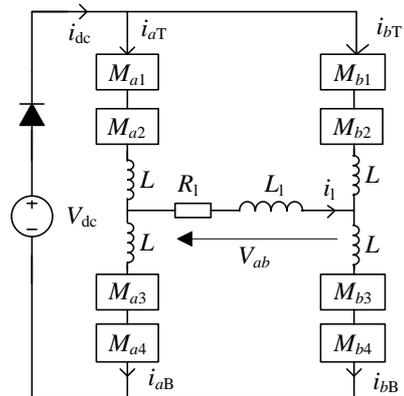
- 6) The candidate switch position with the minimum cost is determined and applied at time-step k .

A receding horizon policy is implemented by repeating these steps at the next sampling instant. Furthermore, additional control objectives, such as dc-link current control, can be easily addressed by adding appropriate terms to the cost function. Prediction horizon can be further extended by using more complicated switching horizons, such as SSE or SESE. Increasing the switching horizon improves the performance of the system, as detailed in [19], [21], [28], and improvement in performance is also expected with the M2LC.

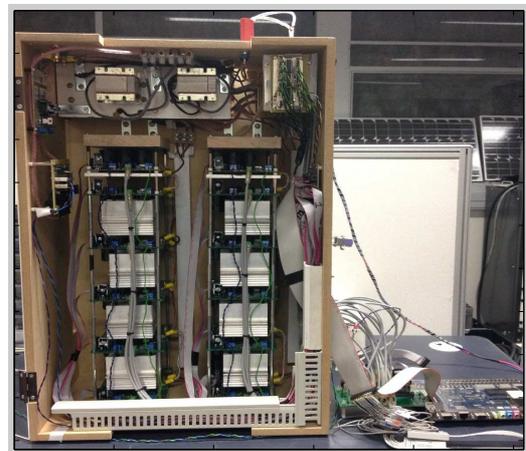
IV. RESULTS

A. M2LC Setup

In order to verify the viability of the proposed MPDCC scheme, a single-phase three-level 860-VA prototype M2LC was constructed. The experimental setup is shown in Fig. 3. The circuit parameters of the system, which are used to verify the performance of the MPDCC through simulations on PLECS/Simulink and experiments, are summarized in Table I. Base quantities for the p.u. system are $V_B = 325.27$ V, I_B



(a) Circuit diagram.



(b) Prototype M2LC.

Fig. 3: Experimental setup of the M2LC.

$= \sqrt{2}I_{rat} = 6.36$ A and $f_B = 50$ Hz. The simulated results are used to benchmark the experimental performance of the MPDCC scheme. The MPDCC algorithm was implemented on a TMS320F28335 Digital Signal Controller (DSC). The DSC has an on-board Analog to Digital Converter (ADC), which was used to measure all the arm, load and dc-link currents and the dc-link and capacitor voltages. Altera's DE2 board was used to generate dead-time for the switching signals of modules and to safely shut down the converter in the unlikely event of a fault. At start-up, a resistor was connected in series with the dc-supply to charge the capacitors and it was bypassed during normal operation of the converter.

MPDCC is computationally demanding, because the trajectories of arm and load currents and capacitor voltages need to be predicted and extrapolated for a maximum number of switch positions, i.e. 36 positions in the single-phase setup. In

TABLE I: System parameters

Parameter		p.u.	SI
Output frequency	f	1	50 Hz
Supply voltage	V_{dc}	1.2298	400 V
Load current	i_1	0.7071	4.5 A
Capacitance	C	27.62	1.72 mF
Load resistance	R_1	0.8217	42 Ω
Load inductance	L_1	0.1537	25 mH
Arm inductance	L	0.0074	1.2 mH

order to solve this problem in a reasonable amount of time, most of the multiplications and divisions were computed offline. This reduces the calculations of the predicted trajectories to a simple logical addition, based on the switching states of the modules, of pre-computed values times the measured state variables.

For example, consider the equation of the predicted load current

$$i_1(k+1) = g(k) - k_1 u_{a1} V_{c,a1}(k) - k_1 u_{a2} V_{c,a2}(k) + k_2 u_{b1} V_{c,b1}(k) + k_2 u_{b2} V_{c,b2}(k) \quad (18)$$

that needs to be evaluated, using for-loops, for all the switching combinations. Here, $g(k) = k_3 V_{dc} + k_4 i_{aT}(k) + k_5 i_{aB}(k) + k_6 i_1(k)$ has to be computed once every sampling interval. Constants k_1 to k_6 depend on the system parameters and are computed offline. The computational time associated with (18) is minimized by replacing multiplicative instructions with a simple predetermined addition that is based on the permitted switching combinations. Two such instructions, which are used for predicting the load current, $i_{1,p}(k+1)$, $p \in \{1, 2, \dots, 36\}$, are presented below:

$$i_{1,1}(k+1) = [g(k)] - [k_1 V_{c,a1}(k)] + [k_2 V_{c,b1}(k)] \quad (19)$$

$$i_{1,2}(k+1) = [g(k)] - [k_1 V_{c,a2}(k)] + [k_2 V_{c,b2}(k)] \quad (20)$$

The terms within square brackets were evaluated once per sampling interval and used throughout the implemented code. Remaining variables, such as arm currents and capacitor voltages were also predicted using the same method. This procedure might increase the required memory size of the DSC, but there is a reduction in computational time from $172 \mu\text{s}$ to $124 \mu\text{s}$. As division operation is computationally expensive, its usage is limited to two: for evaluating the prediction horizon and imposing the penalty on the number of switching transitions in the cost function. The maximum execution time of the MPDCC is $124 \mu\text{s}$, hence a sampling frequency of 8 kHz was chosen. In addition, computational and actuation delay of one sampling interval was compensated by predicting the load current trajectories (14) and finding the candidate positions at $k+2$ instead of $k+1$, as detailed in [29]. The weighting coefficients $\lambda_1 = 0.09$ and $\lambda_2 = 0.36$ were used in the experiments and simulations, and heuristic approach was followed to select their values.

B. Steady-State Performance

At each sampling instant a new switch position was determined over the length of the prediction horizon, where the latter depends upon the bound width, sampling frequency and time constant of the load inductor. As the slope of the load current's ripple changes over a fundamental period, the current trajectory takes a varying amount of time to move within its bounds and thus prediction horizon is dynamic. For the given system parameters and δ of 0.1 p.u., the length of the prediction horizon, in the case of simulations, was in the range of 1 to 150 steps. The relevant aforementioned trajectories were extrapolated for the same length.

Fig. 4 shows both simulated and experimental waveforms of the load current, i_1 , to demonstrate that load currents are

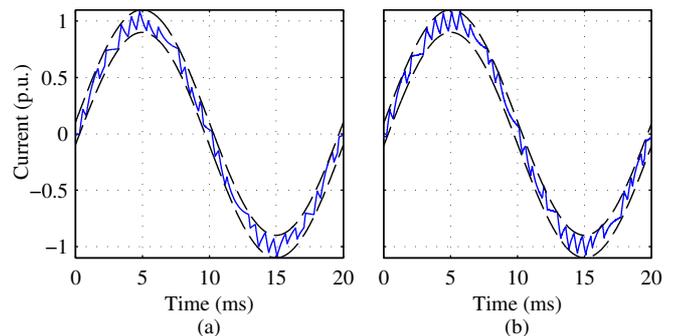


Fig. 4: Waveforms of the load current (a) simulated and (b) experimental. The current band, δ , is 0.1 p.u.

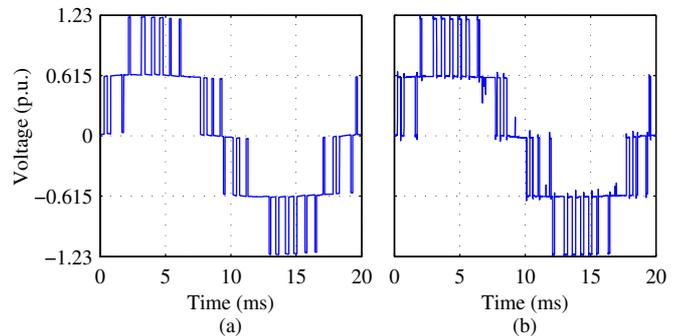


Fig. 5: Waveforms of the output voltage (a) simulated and (b) experimental.

kept inside the bounds. Waveforms of the output voltage, V_{ab} , are shown in Fig. 5. Both simulated and experimental waveforms are similar and confirm the validity of the implemented scheme. All switching transitions appear to take place near the edge of the specified bounds and, at that instant, a new switch position that can minimize the voltage variations and circulating currents was selected. There are few instances where the load current trajectory does not utilize the full bound width. This is because of two reasons: the choice of the weighting coefficients in (17) and increased voltage variations and/or circulating current at that time. The cost function presents a trade-off between the switching frequency or, consequently, utilization of the full bound width and the increased variations of the capacitor voltages and/or circulating currents.

The capacitor voltages were balanced within 4% of their nominal values and Fig. 6 shows the waveforms of the capacitor voltages in phase-leg a for five fundamental periods. Arm currents in phase-leg a and circulating current are shown in Fig. 7. The circulating currents are controlled within 0.15 p.u. of the load currents. Both simulated and experimental waveforms are similar.

THD of the load current and switching frequency of the modules, for a range of bound widths, is shown in Fig. 8. Both the simulations and experiments show a similar trend. Over the range, the THD is a linear function of the bound width. It is evident from Fig. 8 that the THD can be lowered by reducing the bound width, but at a cost of an increased switching frequency. Here, switching frequency was calculated by counting the number of switching transitions of all the modules over a time period of 1 s.

Overall, experimental and simulated results are in good

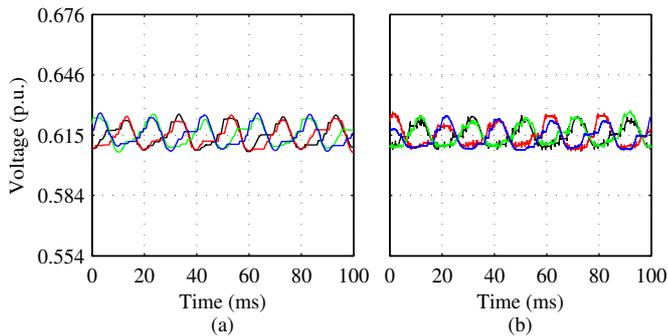


Fig. 6: Waveforms of the capacitor voltages (a) simulated and (b) experimental.

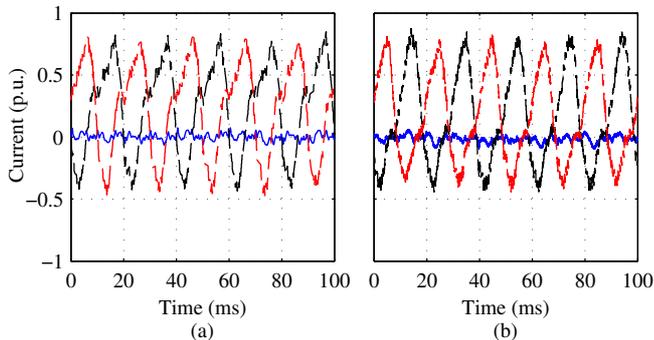


Fig. 7: Waveforms of the arm currents (dashed lines) and circulating current (solid lines) (a) simulated and (b) experimental.

agreement both in values and trend. The discrepancy in the waveforms is due to a number of factors, such as simulations do not consider delays associated with the ADCs and filters. Moreover, the resistive elements that were considered in the simulations, as constant losses, were all estimated values and also add to the slight discrepancy in the waveforms.

C. Performance During Transients

Performance of the MPDCC during transient operating conditions was evaluated under two conditions. Initially, the converter was operating at rated load current before the current reference was changed to zero, termed as power-down, and after 1 s the load current reference was changed back to 1 p.u., termed as power-up. Bound width, $\delta = 0.1$ p.u., of the load current was not changed during the transient operation. Experimental waveforms of the load and arm currents and the capacitor voltages during power-down and power-up transients

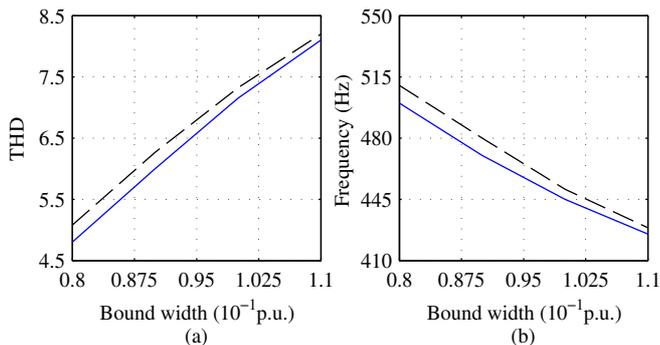


Fig. 8: (a) THD of the load current and (b) switching frequency against the bound width, δ . Dashed and solid lines correspond to the experimental and simulated results, respectively.

are shown in Fig. 9, Fig. 10 and Fig. 11, respectively. To enhance the readability of the time-axis in these figures, the power-down and power-up transients are shown to occur at 20 ms and 10 ms in their respective figures. In the following discussion, only experimental waveforms are presented, because of the space limitation.

The load current, as shown in Fig. 9, takes less than 3 ms to track its reference waveform and has been kept within the specified bounds. The MPDCC achieves a very fast current response both at power-down and power-up. During these transients, the arm currents do not overshoot their steady-state peak values and, as a result, the capacitor voltages do not exhibit large oscillations. The capacitor voltages were kept balanced close to their nominal values. In addition, the capacitor voltages were not rapidly discharged to meet the load, which means that the switch positions were manipulated in a way that the load was supplied by the dc-link.

D. Discussion

At first glance, the cost function (17) seems to have redundant terms, because it has terms for both the voltage variations and circulating currents and these terms are related by (8). Even though the second term in (17) seems sufficient to minimize the variations and the circulating currents, its usage without the third term results in increased circulating currents. This is because of the redundant switching states of the converter, which yield the same output voltage level with minor effect on the output current. These states can be utilized to control the circulating currents. It is possible that a switching state might result in a minimum voltage variation

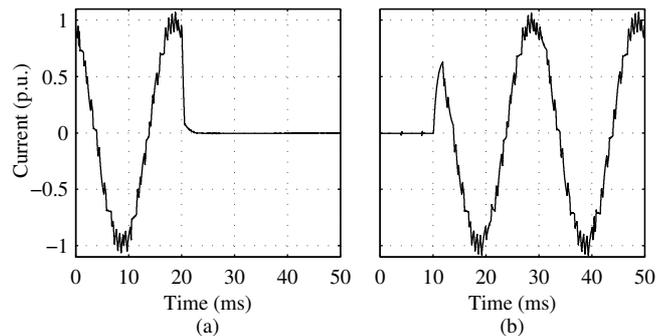


Fig. 9: Experimental waveforms of the load current during (a) power-down and (b) power-up transient.

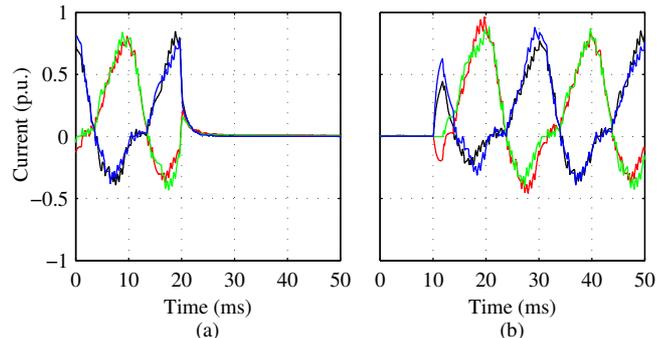


Fig. 10: Experimental waveforms of the arm currents during (a) power-down and (b) power-up transient.

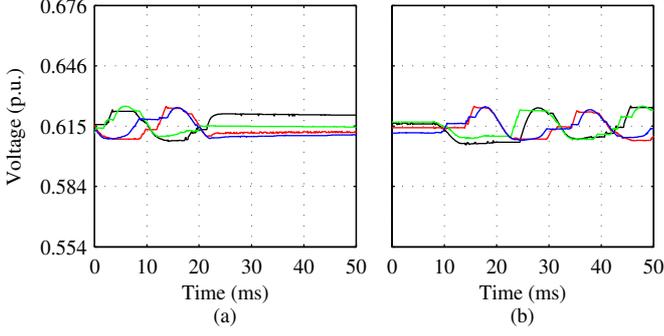


Fig. 11: Experimental waveforms of the capacitor voltages during (a) power-down and (b) power-up transient.

while the same state results in an increased voltage difference in a phase-leg, the right hand side of (8).

For example, consider a M2LC with a dc-link voltage of 400 V and four capacitors per phase-leg that need to be balanced around 200 V. The capacitor voltages are predicted to be 202 V, 199 V, 205 V and 195 V in this hypothetical scenario. From the capacitor balancing perspective, the first two capacitors will be selected, because they are predicted to have minimum voltage variations. On the other hand, voltage difference in a phase-leg will be zero ($400 - 205 - 195 = 0$) with a choice of last two capacitors and is an appropriate choice for minimizing the circulating currents. Selection of sub-optimal states over time results in increased voltage difference in a phase-leg or circulating currents. Therefore, both terms are needed in the cost function.

V. CONCLUSIONS

A model predictive direct current control (MPDCC) scheme, with long prediction horizons, has been proposed for a M2LC with $2N + 1$ line-line voltage levels. It has been shown with both simulations and experiments, using a single-phase three-level 860-VA prototype M2LC, that MPDCC keeps the load current within tight bounds around its sinusoidal reference. It has been demonstrated with experimental results that bounds across the load current determine the THD of the current. Moreover, over a certain range, the THD of the current is a linear function of the degree of bound width. At each sampling instant, the switch position with the minimum cost is applied to the converter. The implemented cost function is a measure of the average switching frequency, capacitor voltage variations and circulating currents. In addition, experimental results also show that the MPDCC achieves an appropriate current response during transient operating conditions. As MPDCC is computationally expensive, most of the calculations were computed offline to reduce the computational burden and a simple yet effective approach has also been proposed to further reduce the computational time.

APPENDIX A SYSTEM MATRICES OF THE FIRST MODEL

$$\mathbf{T} = \begin{bmatrix} L & L & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & L & L & 0 & 0 & 0 \\ -L & -L & -L & -L & 2L & 0 & 0 \\ -L_1 & L + L_1 & L_1 & -L - L_1 & 0 & 0 & 0 \\ 2L_1 & -2L - 2L_1 & L_1 & -L - L_1 & L & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \quad (21)$$

$$\mathbf{F}_i = \begin{bmatrix} -R & -R & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -R & -R & 0 & 0 & 0 \\ R & R & R & R & -2R & 0 & 0 \\ R_1 & -R - R_1 & -R_1 & R + R_1 & 0 & \frac{3}{2} & \frac{-\sqrt{3}}{2} \\ -2R_1 & 2(R + R_1) & -R_1 & R + R_1 & -R & \frac{-3}{2} & \frac{-\sqrt{3}}{2} \\ 0 & 0 & 0 & 0 & 0 & 0 & -\omega \\ 0 & 0 & 0 & 0 & 0 & \omega & 0 \end{bmatrix} \quad (22)$$

$$\mathbf{G}_i = \begin{bmatrix} \mathbf{V}_{aT} & \mathbf{V}_{aB} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{V}_{bT} & \mathbf{V}_{bB} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{V}_{cT} & \mathbf{V}_{cB} \\ \mathbf{0} & \mathbf{V}_{aB} & \mathbf{0} & -\mathbf{V}_{bB} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & -\mathbf{V}_{aB} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{V}_{cB} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \end{bmatrix} \quad (23)$$

with,

$$\mathbf{V}_{rT} = [-V_{c,r1} \quad -V_{c,r2} \quad \dots \quad -V_{c,rN}] \quad (24)$$

$$\mathbf{V}_{rB} = [-V_{c,r(N+1)} \quad -V_{c,r(N+2)} \quad \dots \quad -V_{c,r2N}] \quad (25)$$

$$\mathbf{V}_{dc} = [V_{dc} \quad V_{dc} \quad V_{dc} \quad 0 \quad 0 \quad 0 \quad 0]^T \quad (26)$$

and $\mathbf{0}$ is a zero vector of length N . The parameters used in the above equations are the inductance and resistance of both the load and arm, L_1 , L , R_1 and R , respectively.

APPENDIX B SYSTEM MATRICES OF THE SECOND MODEL

$$\mathbf{F}_c = -\frac{1}{CR_{cap}} \mathbf{I}_{6N} \quad (27)$$

$$\mathbf{G}_c = \frac{1}{C} \begin{bmatrix} i_{aT} \mathbf{I}_N & \mathbf{0}_N & \mathbf{0}_N & \mathbf{0}_N & \mathbf{0}_N & \mathbf{0}_N \\ \mathbf{0}_N & i_{aB} \mathbf{I}_N & \mathbf{0}_N & \mathbf{0}_N & \mathbf{0}_N & \mathbf{0}_N \\ \mathbf{0}_N & \mathbf{0}_N & i_{bT} \mathbf{I}_N & \mathbf{0}_N & \mathbf{0}_N & \mathbf{0}_N \\ \mathbf{0}_N & \mathbf{0}_N & \mathbf{0}_N & i_{bB} \mathbf{I}_N & \mathbf{0}_N & \mathbf{0}_N \\ \mathbf{0}_N & \mathbf{0}_N & \mathbf{0}_N & \mathbf{0}_N & i_{cT} \mathbf{I}_N & \mathbf{0}_N \\ \mathbf{0}_N & \mathbf{0}_N & \mathbf{0}_N & \mathbf{0}_N & \mathbf{0}_N & i_{cB} \mathbf{I}_N \end{bmatrix} \quad (28)$$

Here, $\mathbf{0}_N$ is $N \times N$ zero matrix and \mathbf{I}_{6N} and \mathbf{I}_N are $6N \times 6N$ and $N \times N$ identity matrices, respectively. R_{cap} is used to model the losses associated with the module capacitors.

APPENDIX C
DISCRETE-TIME MATRICES OF THE MODELS

$$\mathbf{A}_i = e^{\mathbf{T}^{-1}\mathbf{F}_i T_s} \quad (29)$$

$$\mathbf{B}_i = \mathbf{F}_i^{-1}\mathbf{T}(\mathbf{A}_i - \mathbf{I}_7)\mathbf{T}^{-1}\mathbf{G}_i \quad (30)$$

$$\mathbf{V}_i = \mathbf{F}_i^{-1}\mathbf{T}(\mathbf{A}_i - \mathbf{I}_7)\mathbf{T}^{-1}\mathbf{V}_{dc} \quad (31)$$

$$\mathbf{C}_i = \begin{bmatrix} 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \\ -1 & 1 & -1 & 1 & 0 \\ \frac{1}{2} & \frac{1}{2} & 0 & 0 & -\frac{1}{3} \\ 0 & 0 & \frac{1}{2} & \frac{1}{2} & -\frac{1}{3} \\ -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} & \frac{2}{3} \end{bmatrix} \quad (32)$$

$$\mathbf{A}_c = e^{\mathbf{F}_c T_s} \quad (33)$$

$$\mathbf{B}_c = \mathbf{F}_c^{-1}(\mathbf{A}_c - \mathbf{I}_{6N})\mathbf{G}_c \quad (34)$$

$$\mathbf{C}_c = \mathbf{I}_{6N} \quad (35)$$

Here, \mathbf{I}_7 and \mathbf{I}_{6N} are 7×7 and $6N \times 6N$ identity matrices, respectively and T_s is the sampling interval.

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