Thermally-Constrained Optimized Pulse Patterns for Medium-Voltage Neutral-Point-Clamped Converters

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Abstract—A method of computing optimized pulse patterns with upper-bounded junction temperatures of semiconductors is presented. An optimization-friendly thermal model with continuous first-order derivatives is derived, which models the junction temperature as a function of the switching angles of a pulse pattern. Expressions for the average, ripple, and instantaneous junction temperatures are derived. By constraining the junction temperature in the optimization problem underlying optimized pulse patterns, pulse patterns that guarantee thermally-safe steady-state operation can be computed. This allows the thermal capabilities of semiconductor to be fully utilized, which typically enables a power increase of the converter system.

Index Terms—Optimized pulse patterns, synchronous optimal pulsewidth modulation, three-level converters, semiconductor losses, semiconductor temperature, medium voltage, optimization

I. INTRODUCTION

Optimized pulse patterns (OPPs)—also known as synchronous optimal pulse-width modulation—are a modulation method where the switching angles are computed offline over a range of modulation indices by solving an optimization problem [1], [2]. The resulting angles are stored in lookup tables. During the operation of a converter system, a modulator reads out the switching angles that correspond with a demanded modulation index [3], [4].

A. Advantages of Optimized Pulse Pattern

When compared to classical modulation schemes, such as carrier-based pulse-width modulation or space-vector modulation, OPPs achieve superior harmonic performanceespecially at low switching frequencies, see [5, Fig. 10]. This is due to the fact that OPPs are typically optimized for minimum harmonic distortions. As a consequence of the lower harmonic distortion, an OPP-modulated converter can operate at low switching frequencies and consequently at low switching losses while still achieving acceptable harmonic distortion levels. Conversely, OPPs reduce the switching losses in a converter system at a given distortion level when compared to classical methods. This makes OPPs particularly attractive for medium-voltage converter systems, where highpower low-switching frequency semiconductor devices, such as integrated gate-commutated thyristors (IGCTs) [6], [7], are used. Furthermore, higher output voltages are easily attained thanks to the seamless extension of OPPs beyond the extended linear modulation regime (up to $m = 2/\sqrt{3} = 1.155$) deep into the nonlinear modulation regime and close to square-wave modulation (with $m = 4/\pi = 1.273$).

B. Thermal Limitations

One of the main quantities that limits the power in a converter system is the junction temperature of the semiconductors. Devices that are conduction-loss optimized tend to have significant switching losses; it is important that the switching instants are carefully selected, since-even if low pulse numbers are adopted—the (peak) device temperatures can easily exceed the safe operating area when commutating high currents. Furthermore, the traditionally used approach of reducing the switching frequency to limit the peak junction temperature should be revisited, because at some point the harmonic distortions will become unacceptably high. Furthermore, it is important to note that the switching frequency serves only as a proxy for the losses, which in turn are a proxy for the peak device temperatures. Thus, attempting to limit the peak temperature by limiting the switching frequencies and/or losses is a suboptimal approach that might result in overly high harmonic distortions.

In order to directly limit the junction temperature, the notion of OPPs needs to be revisited. Since OPPs are computed by solving an optimization problem, the junction temperature can be included in the optimization stage. More specifically, an upper bound on the junction temperature can be enforced via constraints. This results in a well-defined problem formulation: calculate pulse patterns with the lowest possible harmonic distortions while adhering to the thermal limits of the semiconductors.

C. State-of-the-Art Methods to Compute Junction Temperature

Modelling and computing the junction temperature are wellknown in industry, with commercial software packages, such as PLECS, and methods, such as those described in [8], [9], being able to calculate the device temperatures. However, these methods are used to determine the junction temperature profile once a pulse pattern (or any switching sequence) waveform has been made available. Although they could be called by an optimization procedure, their computational burden and lack of closed-form expressions for the temperatures would make calculating the OPPs, for all intents and purposes, computationally intractable. Furthermore, although a moderate amount of literature on active thermal management and thermal estimation is available (see [10], [11]), these methods are embedded in control loops and rely on real-time measurements and, thus, are not applicable to the computation of OPPs.

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Fig. 1: Neutral-point-clamped converter with an active RL load.

D. Proposed Method and Paper Outline

In this paper, an optimization-friendly thermal model of the instantaneous junction temperatures is derived as a function of the switching angle of the to-be-computed pulse pattern. The advantage of the thermal model being an explicit function of the switching angles is that the junction temperatures can be computed in a quick and efficient manner; computationally intensive steps, such as computing the waveforms of the device currents and losses, are not required. Furthermore, expressions for average, ripple, and peak temperatures are available. Importantly, it is shown how to efficiently compute the steadystate temperature. Moreover, the thermal model consists of continuous functions with continuous first-order derivatives. Such first-order derivatives are desired by most-and required by many-gradient-based solvers, such as the open-source IPOPT, to ensure fast convergence and low computation times. To the author's knowledge, this is the first time a method is proposed that enables OPPs to be computed with an upper bounded junction temperature. In summary, our contributions are:

- An efficient and sufficiently accurate model of the instantaneous junction temperature (and also the instantaneous losses) that is an explicit function of the switching angles of an OPP. Thus, a closed-form expression of the junction temperature is obtained.
- For the first time, a method is proposed that limits the junction temperature during optimization of an OPP.

The paper is organized as follow. Sect. II recapitulates OPPs and derives an expression for the output currents. Sects. III and IV derive the expression for switching and conduction losses, respectively. The thermal model is presented in Sect. V, with which the junction temperature can be computed. The model verification and the results of thermally-constrained OPPs are shown in Sect. VI. The paper is concluded in Sect. VII.

As a case study, the (three-level) neutral-point-clamped (NPC) converter is considered, see Fig. 1, which is the workhorse in medium-voltage applications. The converter is considered to be connected to an active resistive-inductive load, such as an electrical machine or grid. The method can readily be adapted to other topologies and/or loads. With only minor loss of generality, assume three-phase symmetry between the three phases; it is thus sufficient to only consider

a single phase of the converter. We denote the single-phase output current and switch position by i and $u \in \{-1, 0, 1\}$, respectively.

II. OPTIMIZED PULSE PATTERNS

OPPs are briefly recapitulated in this section. For a more in-depth overview on OPPs, the reader is referred to [12, Sect. 3.4.3] and [4].

A. Switching Function

In Fig. 2, a three-level pulse pattern u with pulse number d = 3 and its resulting (differential-mode) phase current i are shown. For a three-level pulse pattern, the device switching frequency is given by $f_{sw} = df_1$, where f_1 is the fundamental frequency. We assume that the OPP is, without loss of generality, half-wave symmetric and only switches between 0 and 1 during the first 180° . The (primary) switching angles over 180° are denoted by α_i for $i = 1, 2, \ldots, 2d$. The remaining angles can be calculated as $\alpha_{i+2d} = \alpha_i + \pi$ for $i = 1, 2, \ldots, 2d$. A pulse pattern can be described as

$$u(\theta) = \sum_{i=1}^{4d} \Delta u_i h(\theta - \alpha_i) \tag{1}$$

for $\theta \in [0, 2\pi]$. Here, $h \in \{0, 1\}$ is the unit step function, and $\Delta u_i = u_i - u_{i-1} \in \{-1, 1\}$ is the *i*th switching transition, where $u_i \in \{-1, 0, 1\}$ is the *i*th switch position. Without loss of generality, it is assumed that the initial switch position is $u_0 = 0$.

B. Fourier Analysis

It is common practice to describe the pulse pattern (1) using a Fourier series. It is shown in [13] that a half-wave symmetric pulse pattern can be represented with the Fourier series

$$u(\theta) = \sum_{n=1,3,5,\dots}^{\infty} a_n \cos(n\theta) + b_n \sin(n\theta)$$
(2)



Fig. 2: A half-wave symmetric pulse pattern with pulse number d = 3, the switching angles α_i , and its resulting phase current *i*.

with the coefficients

$$a_n = -\frac{2}{n\pi} \sum_{i=1}^{2d} \Delta u_i \sin(n\alpha_i)$$
(3a)

$$b_n = \frac{2}{n\pi} \sum_{i=1}^{2d} \Delta u_i \cos(n\alpha_i).$$
(3b)

Note that, due to half-wave symmetry, the pulse pattern is sufficiently characterized by the primary switching angles α_i for i = 1, 2, ..., 2d; and its even harmonics are zero.

C. Phase Current

The output phase current of an NPC converter modulated by a pulse pattern can be described as

$$i(\theta, \phi) = i_1(\theta, \phi) + i_h(\theta), \tag{4}$$

where

$$i_1(\theta) = \sqrt{2}I\sin(\theta + \phi) \tag{5}$$

is the fundamental component. The latter depends on the operating point, where I is the rms value of the current and ϕ is the (converter) displacement angle (a positive value indicates that the converter current is leading the converter voltage). The second term in (4) is the harmonic component

$$i_{\rm h}(\theta) = \sum_{n=5,7,11,...}^{\infty} a_{i_{\rm h},n} \cos(n\theta) + b_{i_{\rm h},n} \sin(n\theta),$$
 (6)

which depends on the pulse pattern and system parameters. Note that third-order harmonics are not present in the phase current due to three-phase symmetry and the star point of the load floating. Assuming that the load resistance can be neglected, which is usually the case for medium-voltage systems, the Fourier coefficients of the current harmonics are

$$a_{i_{\rm h},n} = -\frac{v_{\rm dc}}{2\omega_1 L} \frac{b_n}{n} \tag{7a}$$

$$b_{i_{\rm h},n} = \frac{v_{\rm dc}}{2\omega_1 L} \frac{a_n}{n}.$$
 (7b)

Note the load only affects the coefficients of (7); all derivations hereafter are independent of the load. More specifically, for any (linear) load, only (7) requires adaption.

D. Harmonic Current Distortions

It is usually of interest to minimize the harmonic distortions of the phase current *i*. A commonly used metric is the total demand distortion (TDD) of the current, I_{TDD} , which is defined as

$$I_{\rm TDD} = \frac{1}{\sqrt{2}I_{\rm nom}} \sqrt{\sum_{n=5,7,11,\dots} (\hat{i}_n)^2},$$
 (8)

where \hat{i}_n is the amplitude of the *n*th current harmonic, and I_{nom} is the nominal (rms) current. The TDD is proportional to

$$I_{\text{TDD}} \propto \sqrt{\sum_{n=5,7,11,\dots} \frac{(a_n)^2 + (b_n)^2}{(n)^2}},$$
 (9)

which follows from inserting (7) into (8).

E. Optimization Problem

The following (traditional) pulse pattern optimization problem can be formulated to minimize the current TDD:

$$\min_{\alpha_i, \forall i \in \{1, 2, \dots, 2d\}} \sum_{n=5,7,11,\dots} \frac{(a_n)^2 + (b_n)^2}{(n)^2}$$
(10a)

$$0 \le \alpha_1 \le \alpha_2 \le \ldots \le \alpha_{2d} \le \pi \quad (10b)$$

$$m = \frac{2}{\pi} \sum_{i=1}^{\infty} \Delta u_i \cos(\alpha_i)$$
(10c)

$$0 = \frac{2}{\pi} \sum_{i=1}^{2d} \Delta u_i \sin(\alpha_i). \tag{10d}$$

Note that (10b) is required to ensure feasibility of the pulse pattern; (10c) and (10d) follow from the fact that the fundamental component should be equal to the modulation index m and be in phase with a sine wave [see (3) with n = 1].

III. SWITCHING LOSSES

A. Switching Energy Losses

Semiconductors suffer from switching losses due to the noninstantaneous transition times when the device is switching. For GCTs, it is sufficient to assume that the turn-on and turnoff losses linearly depend on the anode-cathode voltage $v_{\rm T}$ and the anode current $i_{\rm T}$. With the device specific coefficients $c_{\rm on}$ and $c_{\rm off}$, the *j*th turn-on and ℓ th turn-off switching energy losses are given by

$$e_{\mathrm{on},j} = c_{\mathrm{on}\,\frac{1}{2}} v_{\mathrm{dc}} i_{\mathrm{T}}(\theta_j, \phi) \tag{11a}$$

$$\varepsilon_{\text{off},\ell} = c_{\text{off}} \frac{1}{2} v_{\text{dc}} i_{\text{T}}(\theta_{\ell},\phi), \qquad (11b)$$

respectively. Note that the anode current $i_{\rm T}$ is, by definition, always positive. For a GCT, $c_{\rm on}$ is typically much smaller than $c_{\rm off}$. Here, the assumption is used that $v_{\rm T} \approx v_{\rm dc}/2$.

The turn-on losses of a diode are close to zero. Therefore, only the turn-off losses—the so-called reverse-recovery losses—are considered. The reverse-recovery losses are assumed to be linear in the voltage but nonlinear in the current, with the kth reverse-recovery energy losses being

$$e_{\mathrm{rr},k} = c_{\mathrm{rr}} \frac{1}{2} v_{\mathrm{dc}} f_{\mathrm{rr}}(i_{\mathrm{T}}(\theta_k, \phi)).$$
(12)





Fig. 3: Conduction paths for a positive phase current (i > 0).

Typically, $e_{\rm rr}$ lies in the interval of $e_{\rm on}$ and $e_{\rm off}$. The nonlinear function $f_{\rm rr}$ is (usually) concave. In case an expression for $f_{\rm rr}$ is not available, a polynomial function can be constructed based on the manufacturers' data points with the help of a least-squares data fitting approach.

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(a) u = -1

 C_{dc}

 $v_{\rm lo}$

In order to calculate the losses, expressions for the current and switching transitions of each device are required. The latter can easily be determined from the single-phase pulse pattern u. In Fig. 3, the conduction paths for positive phase current is shown. The conduction paths for negative current can similarly be determined. The device numbers 1 to 10 are also shown, where the devices 1 to 4 correspond to GCTs, the devices 5 to 8 are freewheeling diodes, and the devices 9 and 10 are clamping diodes.¹ As seen, the devices in the set

$$\{1, 2, 7, 8, 9\}\tag{13}$$

only conduct positive phase current, whereas the devices in the set

$$\{3, 4, 5, 6, 10\}\tag{14}$$

only conduct negative phase current. As an example of the currents through a device, consider Fig. 4, where the current through GCT 1 is shown.

¹In general, we will state the device type before the device index. Device 1, for example, will be referred to as GCT 1, and device 8 will be referred to as Diode 8.

TABLE I: Switching energy losses in an NPC converter.²

Polarity of the current	Switching transition	Switching energy losses	
> 0	$\begin{array}{c} 0 \rightarrow 1 \\ 1 \rightarrow 0 \\ 0 \rightarrow -1 \\ -1 \rightarrow 0 \end{array}$	$\begin{array}{c} e_{\mathrm{on}}^{1}+e_{\mathrm{rr}}^{9}\\ e_{\mathrm{off}}^{1}\\ e_{\mathrm{off}}^{2}\\ e_{\mathrm{on}}^{2}+e_{\mathrm{rr}}^{8} \end{array}$	
< 0	$\begin{array}{c} 0 \rightarrow 1 \\ 1 \rightarrow 0 \\ 0 \rightarrow -1 \\ -1 \rightarrow 0 \end{array}$	$\begin{array}{c} e_{\mathrm{off}}^{3}\\ e_{\mathrm{on}}^{3}+e_{\mathrm{rr}}^{5}\\ e_{\mathrm{on}}^{4}+e_{\mathrm{rr}}^{10}\\ e_{\mathrm{off}}^{4}\end{array}$	



Fig. 4: Current through GCT 1.

In Table I, the switching energy losses for each device is summarized. Note that the polarity of the phase current is required when determining the losses, which is challenging when considering the switching ripple on the phase current.

B. Instantaneous Phase Current Decomposition

To determine the polarity of the phase current (in order to determine when a device carries switching losses), it is useful to decompose the phase current i into its positive and negative components, denoted by i_p and i_n , respectively. Note that the positive and negative components should not be confused with a sequence decomposition of an asymmetrical three-phase signal. So-called extractor functions are thus required that satisfies $g_p(i) \approx 1$ for $i \geq 0$ and $g_p(i) \approx 0$ for i < 0, and $g_n(i) \approx 1$ for i < 0 and $g_n(i) \approx 0$ for $i \geq 0$. Suitable functions for this are the (shifted) hyperbolic tangent functions

$$g_{\rm p}(i) = \frac{1}{2} + \frac{1}{2}\tanh(\lambda i) \tag{15a}$$

$$g_{\rm n}(i) = -\frac{1}{2} + \frac{1}{2} \tanh(\lambda i),$$
 (15b)

²Throughout this paper, superscripts serve as a device label. For example, p_{loss}^3 and T_i^3 refer to the losses and junction temperature, respectively, of GCT 3. In the case that the superscripts refer to an operation, brackets are added. For example, $(x)^2$ implies the square of the variable x.



Fig. 5: Hypberbolic extractor function $g_{\rm p}(i)$ for different λ .



Fig. 6: Extracting the positive and negative phase current components using the hyperbolic extractor function with $\lambda = 60$.

where $\lambda > 0$ is a smoothness factor, see Fig. 5. Note that $g_n = g_p - 1$. Using (15), the positive and negative current components can be extracted using

$$i_{\rm p}(\theta,\phi) = i(\theta,\phi) g_{\rm p}(i(\theta,\phi))$$
 (16a)

$$i_{\rm n}(\theta,\phi) = i(\theta,\phi) g_{\rm n}(i(\theta,\phi)), \tag{16b}$$

respectively. These currents are, by definition, always nonnegative; this implies that the polarity of the negative phase current component is inverted. In particular, the sum of the current components is equal to the absolute value of the phase current, i.e., $|(i(\theta, \phi))| = i_p(\theta, \phi) + i_n(\theta, \phi)$. In Fig. 6, an example of the positive and negative phase current components is shown.

C. Instantaneous Switching Losses

Consider the turn-on switching energy losses of a GCT as defined in (11a). It is well known that the time-derivative of

the energy losses are the power losses; this implies for the turn-on power losses that

$$p_{\rm on}(t) = \frac{\mathrm{d}e_{\rm on}(t)}{\mathrm{d}t} \,. \tag{17}$$

With the substitution $t = \theta/\omega_1$, the power losses can be rewritten as a function of the angle θ ,

$$p_{\rm on}(\theta) = \omega_1 \frac{\mathrm{d}e_{\rm on}(\theta)}{\mathrm{d}\theta}.$$
 (18)

The power losses resulting from a switching event are dissipated within a few microseconds and, thus, instantaneously when considering the time constants of the thermal impedance. This enables the use of impulses to conveniently model the switching power losses. For the *j*th switching transition, the associated turn-on power losses are

$$p_{\mathrm{on},j}(\theta,\phi) = \omega_1 c_{\mathrm{on}} \frac{v_{\mathrm{dc}}}{2} i_{\mathrm{T}}(\theta,\phi) \delta(\theta-\theta_j), \qquad (19)$$

where δ is the well-known impulse function and θ_j is the *j*th switching angle. The impulses are placed at the switching angles where the current is commutated.³ Similarly, for the turn-off and reverse-recovery losses, the switching (power) losses are derived as

$$p_{\text{off},k}(\theta,\phi) = \omega_1 c_{\text{off}} \frac{v_{\text{dc}}}{2} i_{\text{T}}(\theta,\phi) \delta(\theta-\theta_k)$$
(20)

$$p_{\mathrm{rr},\ell}(\theta,\phi) = \omega_1 c_{\mathrm{rr}} \frac{v_{\mathrm{dc}}}{2} f_{\mathrm{rr}}(i_{\mathrm{T}}(\theta,\phi)) \delta(\theta-\theta_\ell), \qquad (21)$$

respectively.

We introduce $c_i \in \{0, c_{\text{on}}, c_{\text{off}}, c_{\text{rr}}\}$ as the switching energy loss coefficient of the *i*th switching transition, which is either zero or captures turn-on, turn-off, or reverse-recovery losses. Furthermore, we define the vector of loss coefficients $\boldsymbol{c} = [c_1 \ c_2 \ \dots \ c_{4d}]^{\text{T}}$, where 4d is the (maximum number) of switching transitions per period. It follows from Table I that

$$\boldsymbol{c}^{\mathrm{T}} = \begin{cases} [c_{\mathrm{on}} \ c_{\mathrm{off}} \ c_{\mathrm{on}} \ \dots \ c_{\mathrm{off}} \ \mathbf{0}_{2d}^{\mathrm{T}}] & \text{for GCT 1,} \\ [\mathbf{0}_{2d}^{\mathrm{T}} \ c_{\mathrm{off}} \ c_{\mathrm{on}} \ c_{\mathrm{off}} \ \dots \ c_{\mathrm{on}}] & \text{for GCT 2,} \\ [c_{\mathrm{off}} \ c_{\mathrm{on}} \ c_{\mathrm{off}} \ \dots \ c_{\mathrm{on}} \ \mathbf{0}_{2d}^{\mathrm{T}}] & \text{for GCT 3,} \\ [\mathbf{0}_{2d}^{\mathrm{T}} \ c_{\mathrm{on}} \ c_{\mathrm{off}} \ c_{\mathrm{on}} \ \dots \ c_{\mathrm{off}}] & \text{for GCT 4,} \\ [\mathbf{0} \ c_{\mathrm{rr}} \ \mathbf{0} \ \dots \ c_{\mathrm{rr}} \ \mathbf{0}_{2d}^{\mathrm{T}}] & \text{for Diode 5,} \\ [\mathbf{0}_{2d}^{\mathrm{T}} \ \mathbf{0} \ c_{\mathrm{rr}} \ \mathbf{0} \ \dots \ c_{\mathrm{rr}}] & \text{for Diode 8,} \\ [c_{\mathrm{rr}} \ \mathbf{0} \ c_{\mathrm{rr}} \ \mathbf{0} \ c_{\mathrm{rr}} \ \mathbf{0} \ \mathbf{0}_{2d}^{\mathrm{T}}] & \text{for Diode 9,} \\ [\mathbf{0}_{2d}^{\mathrm{T}} \ c_{\mathrm{rr}} \ \mathbf{0} \ c_{\mathrm{rr}} \ \dots \ \mathbf{0}] & \text{for Diode 10} \end{cases}$$

The vector $\mathbf{0}_{2d}$ is a zero column vector of dimension 2d.

For the devices of (13), the (commutated) anode current $i_{\rm T}$ is equal to $i_{\rm p}$, whereas for the devices of (14), the anode current is equal to $i_{\rm n}$. To this end, depending on the device,

³It can easily be verified that

$$e_{\mathrm{on},j} = \frac{1}{\omega_1} \int_{-\infty}^{\infty} \omega_1 c_{\mathrm{on}} \frac{v_{\mathrm{dc}}}{2} i_{\mathrm{T}}(\theta,\phi) \delta(\theta-\theta_j) \, \mathrm{d}\theta = c_{\mathrm{on}} \frac{v_{\mathrm{dc}}}{2} i_{\mathrm{T}}(\theta_j,\phi);$$

in other words, the strength of an impulse at the switching instant is equal to the switching energy loss.



Fig. 7: Illustration of the switching loss function p_{sw} for GCT 1.

we define the function z to be either i_p , i_n , $f_{rr}(i_p)$, or $f_{rr}(i_n)$. According to Table I, z is defined as

$$z = \begin{cases} i_{\rm p} & \text{for GCTs } 1, 2, \\ i_{\rm n} & \text{for GCTs } 3, 4, \\ f_{\rm rr}(i_{\rm p}) & \text{for Diodes } 7, 8, 9, \\ f_{\rm rr}(i_{\rm n}) & \text{for Diodes } 5, 6, 10. \end{cases}$$

In case of the GCTs, the function z represents the anode current $i_{\rm T}$; for the diodes, z represents $f_{\rm rr}(i_{\rm T})$.

With these two definitions, the switching losses of a device over a fundamental period can be stated as

$$p_{\rm sw}(\theta,\phi) = \omega_1 \frac{v_{\rm dc}}{2} \sum_{i=1}^{4d} c_i z(\theta,\phi) \delta(\theta - \alpha_i), \qquad (22)$$

where we used the fact that the (potential) switching events of the devices are the switching angles of the pulse pattern. This concept shall be illustrated with an example. Consider GCT 1, which conducts positive phase current and carries switching losses only during the positive halfwave ($0 \le \theta \le \pi$), and assume operation with the pulse pattern shown in Fig. 2. Thus, $z = i_p$ and $c = [c_{on} c_{off} c_{on} c_{off} c_{on} c_{off} \mathbf{0}_{2d}^T]^T$. The resulting switching loss function is shown in Fig 7. Note that at the first switching transition the positive phase current component i_p is zero and, thus, the switching losses are zero as well.

D. Average Switching Losses

The average of a quantity x is defined as

$$x_{\text{avg}} = \frac{1}{2\pi} \int_0^{2\pi} x(\theta) \, \mathrm{d}\theta.$$
 (23)

With this, the average of the switching losses (22) over a period is

$$p_{\rm sw,avg}(\phi) = \omega_1 \frac{v_{\rm dc}}{4\pi} \sum_{i=1}^{4d} c_i z(\alpha_i, \phi).$$
(24)

IV. CONDUCTION LOSSES

The conduction losses are due to the nonzero on-state voltage when a device is in conduction mode. Assume that the on-state voltage

$$v_{\rm on}(\theta) = V_{\rm on} + R_{\rm on} i_{\rm T}(\theta) \tag{25}$$

TABLE II: Conduction power losses in an NPC converter.

Polarity of the current	Switch position	Conduction power losses	
> 0	$ \begin{array}{c} 1 \\ 0 \\ -1 \end{array} $	$\begin{array}{l} p_{\mathrm{cond}}^1 + p_{\mathrm{cond}}^2 \\ p_{\mathrm{cond}}^2 + p_{\mathrm{cond}}^9 \\ p_{\mathrm{cond}}^7 + p_{\mathrm{cond}}^8 \end{array}$	
< 0	$ \begin{array}{c} 1 \\ 0 \\ -1 \end{array} $	$\begin{array}{c} p_{\mathrm{cond}}^5 + p_{\mathrm{cond}}^6 \\ p_{\mathrm{cond}}^3 + p_{\mathrm{cond}}^{10} \\ p_{\mathrm{cond}}^3 + p_{\mathrm{cond}}^4 \end{array}$	

is affine in the current $i_{\rm T}$, where $V_{\rm on}$ denotes the threshold voltage and $R_{\rm on}$ is the slope resistance. These parameters are device-specific.

The (instantaneous) conduction losses for both a GCT and a diode have an identical form, and can be modelled as

$$p_{\text{cond}}(\theta,\phi) = v_{\text{on}}(\theta)i_{\text{T}}(\theta) = V_{\text{on}}i_{\text{T}}(\theta,\phi) + R_{\text{on}}\left(i_{\text{T}}(\theta,\phi)\right)^{2}.$$
(26)

More accurate models can be established, but (26) is sufficient for our purposes. The conduction losses of each device can be derived from Fig. 3 as summarized in Table II.

For the derivation of the conduction losses, the purely sinusoidal phase current

$$i_1(\theta,\phi) = \sqrt{2I}\sin(\theta+\phi) \tag{27}$$

is assumed. By neglecting the current ripple, integrals that do not have closed-form solutions are avoided in subsequent sections. Ignoring the ripple in the conduction loss calculations does not significantly reduce the accuracy of the model because the conduction losses predominantly depend on the fundamental component. This is in contrast to the switching losses, which depend on the instantaneous (commutated) current and, thus, tends to be sensitive to the current ripple.

A. Fundamental Phase Current Decomposition

As with the switching losses, the phase current needs to be decomposed into its positive and negative components. The hyperbolic extractor function (15) cannot be used here, since it would result in integrals that do not have elementary antiderivatives. Instead, the step-based extractor functions

$$g_{1,p}(\theta) = g_0 + \Delta g_1 h(\theta - \phi_1) + \Delta g_2 h(\theta - \phi_2)$$
(28a)

$$g_{1,n}(\theta) = (g_0 - 1) + \Delta g_1 h(\theta - \phi_1) + \Delta g_2 h(\theta - \phi_2)$$
 (28b)

are used to extract the positive and negative phase currents, respectively. Here, $g_0 \in \{0, 1\}$ is the initial extractor position, $\Delta g_i \in \{-1, 1\}$ is the *i*th extractor transition, and ϕ_i is the *i*th extractor transition angle. If the current is positive (negative), $g_{1,p} = 1$ ($g_{1,n} = 1$); otherwise, $g_{1,p} = 0$ ($g_{1,n} = 0$). For a given displacement angle ϕ , the parameters of (28) can easily be determined thanks to the assumption of purely sinusoidal currents. The positive and the (flipped) negative current are

$$i_{1,p}(\theta,\phi) = i_1(\theta,\phi) g_{1,p}(\theta) \tag{29a}$$

$$i_{1,n}(\theta,\phi) = i_1(\theta,\phi) g_{1,n}(\theta), \tag{29b}$$

respectively.



Fig. 8: Extracting the positive and negative phase current using the step-based extractor function.

For an illustration of the extractor function, refer to Fig. 8. Note that the extractor transitions angles ϕ_i are set equal to the zero crossing angles of the phase currents. In the figure, in which $0 \le \phi \le \pi$ holds, the extractor transitions angles are set to $\phi_1 = \pi - \phi$ and $\phi_2 = 2\pi - \phi$.

Note that (29) can be expanded to the second power of the current as

$$(i_{1,p}(\theta,\phi))^2 = (i_1(\theta,\phi))^2 g_{1,p}(\theta)$$
 (30a)

$$(i_{1,n}(\theta,\phi))^2 = -(i_1(\theta,\phi))^2 g_{1,n}(\theta).$$
 (30b)

This property will be required in the next section when computing the conduction losses.

B. Instantaneous Conduction Losses

The switching state of any device can be described by

$$s(\theta) = \sum_{i=0}^{4d} \Delta s_i h(\theta - \alpha_i), \qquad (31)$$

where $s \in \{0, 1\}$. If s = 1, the device conducts; likewise, if s = 0, the device is in the blocking state. Note that the sum in (31) starts with the index i = 0, with the dummy switching angle and switching state transition defined as $\alpha_0 = 0$ and $\Delta s_0 = s_0$, respectively. The switching state transitions $\Delta s_i \in \{-1, 0, 1\}$ are a function of the specific device and the pulse pattern. Let $\Delta s = [s_0 \ \Delta s_1 \ \Delta s_1 \ \dots \ \Delta s_{4d}]^T$ denote the vector

of switching transitions. The vector Δs is defined for each device as

$$\Delta \boldsymbol{s}^{\mathrm{T}} = \begin{cases} [0 \ 1 \ -1 \ 1 \ \dots \ -1 \ \boldsymbol{0}_{2d}^{\mathrm{T}}] & \text{for GCT 1, Diodes 5, 6,} \\ [1 \ \boldsymbol{0}_{2d}^{\mathrm{T}} \ -1 \ 1 \ -1 \ \dots \ 1] & \text{for GCT 2,} \\ [1 \ -1 \ 1 \ -1 \ \dots \ 1 \ \boldsymbol{0}_{2d}^{\mathrm{T}}] & \text{for GCT 3,} \\ [0 \ \boldsymbol{0}_{2d}^{\mathrm{T}} \ 1 \ -1 \ 1 \ \dots \ -1] & \text{for GCT 4, Diodes 7, 8,} \\ [1 \ -1 \ 1 \ -1 \ \dots \ 1] & \text{for Diodes 9, 10.} \end{cases}$$
(32)

With this, according to Table II, the anode current can be expressed as

$$\begin{aligned} \dot{v}_{\rm T}(\theta,\phi) &= s(\theta) \begin{cases} i_{1,\rm p}(\theta,\phi) & \text{for GCTs 1, 2, Diodes 7, 8, 9,} \\ i_{1,\rm n}(\theta,\phi) & \text{for GCTs 3, 4, Diodes 5, 6, 10} \\ &= s(\theta) \begin{cases} g_{1,\rm p}(\theta,\phi) \\ g_{1,\rm n}(\theta,\phi) \end{cases} \end{cases} i_1(\theta,\phi), \end{aligned}$$

$$(33)$$

where (29) has been used. Using (28) we define the variable

$$r(\theta) = \bar{g}_0 + \Delta g_1 h(\theta + \phi_1) + \Delta g_2 h(\theta + \phi_2)$$

with

$$\bar{g}_0 = \begin{cases} g_0 & \text{for GCTs 1, 2, Diodes 7, 8, 9,} \\ g_0 - 1 & \text{for GCTs 3, 4, Diodes 5, 6, 10.} \end{cases}$$
(34)

This simplifies (33) to

$$i_{\rm T}(\theta,\phi) = s(\theta)r(\theta)i_1(\theta,\phi).$$
(35)

Similarly, the squared anode current is defined as

$$(i_{\mathrm{T}}(\theta,\phi))^2 = bs(\theta)r(\theta)(i_1(\theta,\phi))^2, \qquad (36)$$

where the auxiliary variable

$$b = \begin{cases} 1 & \text{for GCTs 1, 2, Diodes 7, 8, 9,} \\ -1 & \text{for GCTs 3, 4, Diodes 5, 6, 10} \end{cases}$$
(37)

has been introduced, see also (30).

The anode current can now be stated as a function of the switching angles, switching transitions, and phase current. To this end, we insert (27) and (31) into (35) to obtain the anode current, and insert the same equations into (36) to derive the squared anode current. This leads to

$$i_{\rm T}(\theta,\phi) = \sum_{i=0}^{4d} \Delta s_i h(\theta - \alpha_i) \left(\bar{g}_0 + \Delta g_1 h(\theta - \phi_1) + \Delta g_2 h(\theta - \phi_2)\right) \sqrt{2} I \sin(\theta + \phi)$$
(38a)
$$i_{\rm T}(\theta,\phi))^2 = \sum_{i=0}^{4d} \Delta s_i h(\theta - \alpha_i) \left(\bar{g}_0 + \Delta g_1 h(\theta - \phi_1) + \Delta g_2 h(\theta - \phi_2)\right) b2(I)^2 (\sin(\theta + \phi))^2.$$
(38b)

Let

(

 $\boldsymbol{\alpha} = [0 \ \alpha_1 \ \alpha_2 \ \cdots \ \alpha_{4d}]^{\mathrm{T}}$

denote the augmented vector of switching angles over a fundamental period. Recall that $\alpha_0 = 0$ is a dummy switching angle introduced in (31). The product of two step functions at

the angles ξ and ζ is the step function at the maximum of the two angles, i.e.,

$$h(\theta - \xi)h(\theta - \zeta) = h(\theta - \max(\xi, \zeta)).$$

With this, the sum in (38) is rewritten as

$$\sum_{i=0}^{4d} \Delta s_i h(\theta - \alpha_i) \left(\bar{g}_0 + \Delta g_1 h(\theta - \phi_1) + \Delta g_2 h(\theta - \phi_2) \right) = \sum_{i=0}^{12d+2} \Delta \bar{s}_i h(\theta - \bar{\alpha}_i) , \qquad (39)$$

where we have made two definitions. The first one is the auxiliary vector of switching angles

$$ar{oldsymbol{lpha}} = egin{bmatrix} oldsymbol{lpha}^{\mathrm{T}} & \max\{oldsymbol{lpha}^{\mathrm{T}}, \phi_1\} & \max\{oldsymbol{lpha}^{\mathrm{T}}, \phi_2\} \end{bmatrix}^{\mathrm{T}},$$

which uses componentwise maximum operations and is of the dimension 3(4d + 1). The multiplier 3 results from the fact that the sum in (39) involves three products of step functions, whereas 4d + 1 is the dimension of the augmented vector of switching angles. The second definition is the auxiliary vector of switching state transitions

$$\Delta \bar{\boldsymbol{s}} = \begin{bmatrix} \Delta \boldsymbol{s}^{\mathrm{T}} \bar{g}_{0} & \Delta \boldsymbol{s}^{\mathrm{T}} \Delta g_{1} & \Delta \boldsymbol{s}^{\mathrm{T}} \Delta g_{2} \end{bmatrix}^{\mathrm{T}}$$

Inserting (38) with the definition (39) into the conduction losses (26) leads to the closed-form expression

$$p_{\text{cond}}(\theta,\phi) = \sum_{i=0}^{12d+2} \Delta \bar{s}_i h(\theta - \bar{\alpha}_i) \left(\sqrt{2} V_{\text{on}} I \sin(\theta + \phi) + b2R_{\text{on}}(I)^2 \left(\sin(\theta + \phi)\right)^2\right)$$
(40)

for the conduction losses.

Equation (40) consists of products of step functions and sine (and squared sine) functions. We define the sum of step-like sine functions as

$$\nu(\theta,\phi) = \sum_{i=0}^{12d+2} \Delta \bar{s}_i h(\theta - \bar{\alpha}_i) \sin(\theta + \phi), \qquad (41)$$

and the sum of step-like squared sine functions as

$$\mu(\theta,\phi) = \sum_{i=0}^{12d+2} \Delta \bar{s}_i h(\theta - \bar{\alpha}_i) \left(\sin(\theta + \phi)\right)^2.$$
(42)

With this, the conduction losses (40) can be stated in the compact form

$$p_{\text{cond}}(\theta,\phi) = \sqrt{2}V_{\text{on}}I\nu(\theta,\phi) + b2R_{\text{on}}(I)^2\mu(\theta,\phi).$$
(43)

Refer to Fig. 9 for an illustration of the conduction loss function for GCT 1 when using the pulse pattern shown in Fig. 2. GCT 1 switches only for $0 \le \theta \le \pi$, and it conducts during the positive half-wave of the phase current. From (32), we obtain $\Delta s = [0 \ 1 \ -1 \ 1 \ -1 \ 0 \ 2_{d}]^{\mathrm{T}}$, from (34), we deduce $\bar{g}_0 = g_0$, and (37) states that b = 1.



Fig. 9: Illustration of the conduction loss function p_{cond} for GCT 1.

C. Average Conduction Losses

Using (23), the average conduction losses of (43) are

 $p_{\rm cond,avg}(\phi) = \sqrt{2}V_{\rm on}I\nu_{\rm avg}(\phi) + b2R_{\rm on}(I)^2\mu_{\rm avg}(\phi), \quad (44)$ where

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$$\nu_{\text{avg}}(\phi) = \frac{1}{2\pi} \sum_{i=0}^{12d+2} \Delta \bar{s}_i (\cos(\bar{\alpha}_i + \phi) - \cos(\phi))$$
(45a)
$$\mu_{\text{avg}}(\phi) = \frac{1}{8\pi} \sum_{i=0}^{12d+2} \Delta \bar{s}_i (\sin(2\bar{\alpha}_i + 2\phi) - 2\bar{\alpha}_i - \sin(2\phi) + 4\pi).$$
(45b)

V. MODELING AND CONSTRAINING THE JUNCTION TEMPERATURE

A. Thermal Model

We adopt the Foster model as thermal model of the semiconductor junction temperatures. As shown in Fig. 10, the model consists of *n* resistor-capacitor elements that model the heat transfer from the semiconductor junction through its case and heat sink to the cooling water. As such, the Foster model determines the steady-state (and transient) junction-to-water temperature drop T_{j-w} between the semiconductor junction and the cooling water.⁴ Defining the temperature of the cooling water as T_w , the junction temperature of a semiconductor device is given by

$$T_{j} = T_{j-w} + T_{w}.$$
(46)

The input to the thermal model are the (instantaneous) total losses of a semiconductor

$$p_{\text{loss}}(\theta, \phi) = p_{\text{sw}}(\theta, \phi) + p_{\text{cond}}(\theta, \phi), \quad (47)$$

which are the sum of the switching and conduction losses. In the frequency domain, the thermal model is given by

$$T_{j-w}(s,\phi) = P_{loss}(s,\phi)Z_{TH}(s), \qquad (48)$$

where s is the complex variable, and

$$Z_{\rm TH}(s) = \sum_{i=1}^{n} \frac{R_i}{\tau_i s + 1}$$

is the transient thermal impedance with the time constants $\tau_i = R_i C_i$.

 $^{4}\mathrm{In}$ case of air-cooled semiconductors, the junction-to-ambient $T_{\rm j-a}$ temperature can be used.



Fig. 10: Foster thermal model of *n*th order of the heat transfer from the semiconductor junction through its case and heat sink to the cooling water.

In the time-domain, the Foster model can be described with n differential equations and an output equation. The model is written in the state-space form as

$$\frac{\mathrm{d}\boldsymbol{T}(\boldsymbol{\theta},\boldsymbol{\phi})}{\mathrm{d}\boldsymbol{\theta}} = \boldsymbol{F}\boldsymbol{T}(\boldsymbol{\theta},\boldsymbol{\phi}) + \boldsymbol{G}p_{\mathrm{loss}}(\boldsymbol{\theta},\boldsymbol{\phi}) \tag{49a}$$

$$T_{j-w}(\theta,\phi) = \mathbf{1}_n^{\mathrm{T}} \boldsymbol{T}(\theta,\phi)$$
(49b)

with the state vector

$$\boldsymbol{T}(\theta,\phi) = \begin{bmatrix} T_1(\theta,\phi) & T_2(\theta,\phi) & \cdots & T_n(\theta,\phi) \end{bmatrix}^{\mathrm{T}}$$
(50)

and the system and input matrices

$$\boldsymbol{F} = \begin{bmatrix} -\frac{1}{\tau_1} & 0 & \cdots & 0\\ 0 & -\frac{1}{\tau_2} & \cdots & 0\\ \vdots & & \ddots & \vdots\\ 0 & 0 & \cdots & -\frac{1}{\tau_n} \end{bmatrix} \frac{1}{\omega_1} \text{ and } \boldsymbol{G} = \begin{bmatrix} \frac{1}{C_1} \\ \frac{1}{C_2} \\ \vdots\\ \frac{1}{C_n} \end{bmatrix} \frac{1}{\omega_1}.$$
(51)

Here, $\mathbf{1}_n \in \mathbb{Z}^n$ is a vector of ones. The angular fundamental frequency ω_1 emerges by formulating the state-space model with respect to the angle θ rather than the time t.

Since water-cooled devices with a strong water flow are adopted in this work, the effect of cross-coupling is negligible and therefore ignored. Note that this is not at the expense of generality of the proposed method. In the case that crosscoupling between devices is required for sufficient accuracy, a Foster model with cross-coupling can be used. Alternatively, the Cauer model may also be used, which has a (physical) representation of the semiconductor layers and its interaction with the cooling system, see [14]. Regardless of whether a Foster model with cross-coupling or the Cauer model is chosen, a linear state-space representation is obtained (and no modifications are required to the proposed method).

B. Average Temperature

Calculating the average junction-to-water temperature drop $T_{j-w,avg}$ is straightforward; it can be found by setting s = 0 rad/s in (48), resulting in

$$T_{j-w}(0,\phi) = P_{loss}(0,\phi)Z_{TH}(0),$$
 (52)

where

$$Z_{\rm TH}(0) = \sum_{i=1}^{n} R_i.$$
 (53)

Thus, the dc-component (or average value) of the steady-state temperature drop is

$$T_{j-w,avg}(\phi) = p_{loss,avg}(\phi) \sum_{i=1}^{n} R_i$$
(54)

with the average switching and conduction losses defined in (24) and (44), respectively.

C. Instantaneous Temperature

One well-known way to calculate the instantaneous junction-to-water temperature drop during steady-state operation is to use a Fourier series. However, this requires summing up a finite number of harmonics; the more harmonics are considered, the more accurate the Fourier series representation will be. Due to the truncation of the sums, the Fourier series suffers from the so-called Gibbs phenomenon, which—during numerical optimization—may lead to numerical inaccuracies. Note that the impulse-like nature of the switching losses causes a step-like response in the temperature, which would require a very large number of harmonics to minimize the Gibbs phenomenon. This implies a trade-off between accuracy and computational burden.

Instead, we propose to calculate the instantaneous temperature drop during steady-state operation by finding the steadystate solution of the differential equations. More specifically, by integrating (49a), the temperature state vector at the angle θ is

$$\boldsymbol{T}(\theta,\phi) = \boldsymbol{e}^{\boldsymbol{F}\theta}\boldsymbol{T}(0,\phi) + \int_0^\theta \boldsymbol{e}^{\boldsymbol{F}(\theta-\vartheta)}\boldsymbol{G}p_{\text{loss}}(\vartheta,\phi) \,\,\mathrm{d}\vartheta \quad (55)$$

with the (unknown) initial temperature state vector $T(0, \phi)$. To compute the latter we note that the temperature is 2π -periodic during steady-state operation, i.e.,

$$\boldsymbol{T}(0,\phi) = \boldsymbol{T}(2\pi,\phi).$$

This observation allows us to compute the initial temperature state vector $T(0, \phi)$, based on which the (steady-state) temperature state vector $T(\theta, \phi)$ at the arbitrary angle $\theta \in [0, 2\pi]$ can be determined; the required computational steps are derived in detail in the appendix. The junction-to-water temperature drop then directly follows from (49b) as

$$T_{\mathbf{j}-\mathbf{w}}(\theta,\phi) = \sum_{i=1}^{n} T_i(\theta,\phi).$$
(56)

The proposed method allows us to compute the junction temperature in a precise and computationally efficient manner at any angle θ . Numerical inaccuracies, which are an inherent drawback of the classic Fourier series approach mentioned above, are avoided.

D. Temperature Ripple

The ripple on the junction-to-water temperature drop is defined as the instantaneous minus the average temperature drop, i.e.,

$$T_{j-w,rip}(\theta,\phi) = T_{j-w}(\theta,\phi) - T_{j-w,avg}(\phi).$$
(57)

Recall that the instantaneous and the average temperature drops are given by (56) and (54), respectively.



Fig. 11: Temperature constraint on the instantaneous junction temperature of GCT 1 for pulse number d = 2.

E. Constraining the Semiconductor Temperature

Denote with T_{j-w}^j the junction-to-water temperature drop of the *j*th device. Denote with \mathcal{D} the set of relevant displacement angles and with $\mathcal{J} \subseteq \{1, 2, \ldots, 10\}$ the index set of devices that are considered. There are a variety of ways the junction temperature can be constrained. Namely, the average, the ripple, and/or the peak temperatures can be constrained.

For the average junction temperature, the constraints are of the form

$$T_{j-w,avg}^{j}(\phi) + T_{w} \le T_{avg,lim}^{j}, \ \forall j \in \mathcal{J}, \forall \phi \in \mathcal{D}.$$
 (58)

Similarly, the ripple or the peak (instantaneous) temperature can be constrained by

$$\left| T_{j-w,rip}^{j}(\theta,\phi) \right| \leq T_{rip,lim}^{j}, \ \forall j \in \mathcal{J}, \forall \theta \in \mathcal{A}^{j}, \forall \phi \in \mathcal{D}, \ (59)$$

$$T_{j-w}^{j}(\theta,\phi) + T_{w} \leq T_{\lim}^{j}, \ \forall j \in \mathcal{J}, \forall \theta \in \mathcal{A}^{j}, \forall \phi \in \mathcal{D},$$
(60)

respectively. These constraints are added to the optimization problem (10). Note that, due to the high switching losses of medium-voltage converters, it is highly likely that the peaks of the ripple and instantaneous temperatures occur at a switching transition. For this reason, these constraints are imposed at the device-specific angle sets $\mathcal{A}^j \subseteq \{\alpha_1, \alpha_2, \ldots, \alpha_{4d}\}$. If needed, additional constraints at intermediate angles could be considered as well.

Fig. 11 illustrates the peak constraint on the junction temperature of GCT 1 for pulse number d = 2 and the (lagging) displacement angle $\phi = -30^{\circ}$. The black dots represent the switching angles at which the temperature is constrained; these are the switching angles in the set $\mathcal{A}^1 = \{\alpha_1, \alpha_2, \alpha_3, \alpha_4\}$, which correspond to the switching angles in the first 180° of the fundamental period.

VI. VERIFICATION AND RESULTS

A 13.7 MVA grid-connected converter system is considered that is operated at the fundamental frequency of 50 Hz; the nominal modulation index is m = 1.11. The typical parameters of such a systems are shown in Table III.

As semiconductors, the 5SHY 55L4500 asymmetric IGCT [15] and the 5SDF 20L4520 fast-recovery diode [16] are used; both were developed by ABB and are now manufactured by Hitachi Energy. The relevant parameters of the semiconductors and their thermal models are summarized in Table IV. The

TABLE III: Parameters of the medium-voltage converter system

Parameter	Symbol	SI values	
Rated power Rated voltage Rated current Rated frequency Dc-link voltage Half dc-link capacitance	$S_{ m R}$ $V_{ m R}$ $I_{ m R}$ f_1 $V_{ m dc}$ $C_{ m dc}$	13.72 MVA 3300 V 2400 A 50 Hz 4840 V 22 mF	
Load inductance Load resistance	L R	$0.51\mathrm{mH}$ $7.9\mathrm{m}\Omega$	

values of the on-state threshold voltage $V_{\rm on}$ and slope resistance $R_{\rm on}$ result from a linearisation of the on-state voltage at $i_{\rm T} = \sqrt{2}I_{\rm R}$. The coefficients $c_{\rm on}$, $c_{\rm off}$, and $c_{\rm rr}$ are based on the losses at $i_{\rm T} = \sqrt{2}I_{\rm R}$, $v_{\rm T} = V_{\rm dc}/2$, and $T_{\rm j} = T_{\rm j,max}$. The coefficient $c_{\rm rr}$ is calculated by defining $f_{\rm rr}$ such that $f_{\rm rr}(\sqrt{2}I_{\rm R}) = \sqrt{2}I_{\rm R}$. The maximum loss values are used, which are roughly 20% higher than the typical values.

The switching and conduction losses at the maximum allowed junction temperature (125 °C for the GCTs, 140 °C for the diodes) are shown in Fig. 12 as a function of the current. For the switching losses, it is assumed that $v_{\rm T} = V_{\rm dc}/2$. The cooling water temperature is $T_{\rm w} = 37$ °C unless mentioned otherwise.

Throughout this section, only the semiconductors in the upper half of the converter will be considered. The losses and junction temperatures of the semiconductors in the lower half are the same as those in the upper half, albeit phase-shifted by 180° due to the fact that the OPPs under consideration always impose (at least) half-wave symmetry. Moreover, Diode 6 has the same conduction losses as Diode 5, see Table II, but incurs

TABLE IV: Parameters of the semiconductors.

Parameter	Symbol	SI values		
IGCT 5SHY 55L4500				
Maximum junction temperature Maximum (rms) current On-state threshold voltage On-state slope resistance Turn-on coefficient Turn-off coefficient	$T_{ m j,max}$ $I_{ m T,max}$ $V_{ m on}$ $R_{ m on}$ $c_{ m off}$	125 °C 2940 A 1.22 V 0.28 mΩ 0.16 μs 2.80 μs		
Junction-to-case thermal model Thermal resistances Time constants	$R_{1-4} = \tau_{1-4}$	$\begin{array}{c} 5.56, 1.53, 0.87, 0.55\mathrm{K/kW} \\ 512, 89.6, 9.1, 2.4\mathrm{ms} \end{array}$		
Case-to-water thermal model	_			
Thermal resistances Time constants	R_{5-6} $ au_{5-6}$	$7.0, 2.4 \mathrm{K/kW}$ 9000, 3000 ms		
Diode	Diode 5SDF 20L4520			
Maximum junction temperature Maximum (rms) current On-state threshold voltage On-state slope resistance Reverse-recovery coefficient	$T_{ m j,max}$ $I_{ m T,max}$ $V_{ m on}$ $R_{ m on}$ $c_{ m rr}$	$\begin{array}{c} 140\ ^{\circ}\mathrm{C} \\ 3100\ \mathrm{A} \\ 1.7\ \mathrm{V} \\ 0.8\ \mathrm{m}\Omega \\ 1.38\ \mathrm{\mu}\mathrm{s} \end{array}$		
Junction-to-case thermal model	-			
Thermal resistances Time constants	$\begin{array}{c} R_{1-4} \\ \tau_{1-4} \end{array}$	$\begin{array}{c} 3.71, 1.43, 0.69, 0.18\mathrm{K/kW} \\ 534, 67.0, 7.4, 1.1\mathrm{ms} \end{array}$		
Case-to-water thermal model	_			
Thermal resistances Time constants	R_{5-6} $ au_{5-6}$	$\begin{array}{c} 2.5, 10.4{\rm K/kW} \\ 4000, 8000{\rm ms} \end{array}$		



Fig. 12: Semiconductor losses according to the manufacturer's model.

no reverse-recovery losses, see Table I. Therefore, it suffices to consider GCTs 1 and 2, and Diodes 5 and 9.

It should be stressed that the effectiveness of our modelbased methods strongly depends on how accurately the utilized semiconductor can be characterized. In this paper, which focuses on presenting a new method, it is assumed that the underlying semiconductors have been accurately modelled and parameterized.

A. Model Verification

To investigate the effect of our assumptions that were made during the derivation of our thermal model, we compare the derived junction temperatures with a PLECS simulation. PLECS considers the ripples on the dc-link voltage and the phase currents when computing the switching and conduction losses. In particular, the switching losses are obtained from 3d look-up tables with the (instantaneous) device current, blocking voltage, and junction temperature as the inputs. The on-state voltage is obtained by a 2d look-up table with the (instantaneous) device current and junction temperature as the inputs. These look-up tables are provided by the manufacturer.

In contrast, our thermal model relies on several approximations and simplifications (which are not present in PLECS):

- The ripple on the dc-link voltage is ignored and the dclink midpoint, the neutral-point potential, is zero. The ripple in the blocking voltage is usually around 50 V to 100 V, which only results in minor inaccuracies.
- Sinusoidal currents are assumed for the conduction losses (whereas the current ripple is included when computing



Fig. 13: Switching angles of the half-wave symmetric OPP with d = 3 but without thermal constraints.

the switching losses). The current ripple is small to moderate, with the current TDD being typically close to 10%, which is well tolerated and only causes minor inaccuracies at the rated current.

- The reverse-recovery function f_{rr} is approximated with a fourth-order polynomial.
- The on-state voltage is affine in the current (linear plus an offset), see (25). The linear term results from a linearization at the rated current, so it is accurate at high currents.
- The losses are characterized assuming the semiconductors are operated at their thermal limits; the temperature-dependence of the losses is neglected to avoid a nonlinear system.

The simplification of ignoring the temperature-dependence of the losses may be justified by the fact that we require our thermal model to be particularly accurate when operating close to the thermal limits. When operating at low junction temperatures, however, the thermal constraints are inactive and modeling errors in the thermal model can be tolerated. For this reason, when comparing our thermal model with the PLECS simulation, we ensure that each device is operated close to its thermal limit. To achieve this, we adjust the (hypothetical) water temperature of each device so that the average junction temperature of each device is $T_{j,avg} = T_{j,max} - 10$ °C.

Six different displacement angles are considered, i.e., $\phi \in \{-210^\circ, -180^\circ, -150^\circ, -30^\circ, 0^\circ, 30^\circ\}$. The converter is operated at its rated current $I_{\rm R}$ using the half-wave symmetric OPP with pulse number d = 3 and without thermal constraints, whose switching angles are shown in Fig. 13. The PLECS simulations are run until a thermal steady-state has been reached. The results are summarized in Table V, which shows the differences between the maximum (instantaneous) junction temperatures obtained with our thermal model and the PLECS simulations. In Fig. 14, the instantaneous temperatures at $\phi = 0^\circ$ are shown.

The differences in temperatures are mostly due to an offset in the average losses. According to these results, the thermal model is accurate within $3.5 \,^{\circ}\text{C}$ (and mostly within $2 \,^{\circ}\text{C}$), which is sufficient for the purpose of computing thermally-



Fig. 14: Junction temperatures of the derived thermal model versus a PLECS simulation when operating close to $T_{j,max}$.



Fig. 15: GCT 1's junction temperature of the derived thermal model versus a PLECS simulation when operating below $T_{j,max}$.

constrained OPPs. The (relatively small) inaccuracies of the thermal model can be attributed to the approximations and simplifications made when deriving the thermal model, as discussed at the beginning of this section.

To illustrate that the thermal model is not accurate at lower junction temperatures, for example, we adjust the current to 50% of its rated value. This results in $T_{j,avg} \approx 70$ °C. Note that the grid voltage is adjusted so that the pulse pattern as well remains identical to that of Fig. 14. The instantaneous junction temperature of GCT 1 is shown in Fig. 15. As can be seen, our thermal model overestimates the junction temperature by 4.9 °C; in contrast, in Fig 14(a), the junction temperature is overestimated by 2.5 °C. This is due to our loss model being characterized at $T_{j,max}$, where the losses are at their highest. As mentioned earlier, inaccuracies when operating below $T_{j,max}$ are not a problem for our proposed method, since the thermal constraints will be inactive during optimization.

TABLE V: Maximum differences in the instantaneous junction temperatures between the thermal model and the PLECS simulations. A positive value indicates that the thermal model calculated a higher temperature than PLECS.

	Displacement angle ϕ					
	-210°	-180°	-150°	-30°	0°	30°
GCT 1 GCT 2 Diode 5	$0.0 ^{\circ}\text{C}$ -0.9 $^{\circ}\text{C}$ -3.5 $^{\circ}\text{C}$	$0.0 ^{\circ}\text{C}$ $1.2 ^{\circ}\text{C}$ $0.4 ^{\circ}\text{C}$	$0.3 ^{\circ}\mathrm{C}$ $0.2 ^{\circ}\mathrm{C}$ $-1.2 ^{\circ}\mathrm{C}$	$0.8 ^{\circ}\mathrm{C}$ $0.4 ^{\circ}\mathrm{C}$ $0.5 ^{\circ}\mathrm{C}$	2.5 °C 1.1 °C 0.0 °C	-1.1 °C -1.1 °C 0.1 °C
Diode 9	$-1.0^{\circ}{ m C}$	$-0.1^{\circ}{ m C}$	0.0 °C	$0.2^{\circ}\mathrm{C}$	$1.9^{\circ}\mathrm{C}$	$-1.3^{\circ}{\rm C}$

B. OPPs without Thermal Constraints

As before, the converter is operated at its rated current $I_{\rm R}$ with displacement angles $-30^{\circ} \le \phi \le 30^{\circ}$ and $-210^{\circ} \le \phi \le -150^{\circ}$. Modulation indices between 0.85 and 1.23 are considered. Lower modulation indices are not investigated, since they are usually not required during steady-state operation of a grid-connected converter.

In a first step, OPPs without thermal constraints are considered. The pulse number is set to d = 3, which results in a device switching frequency of $f_{sw} = 150$ Hz. OPPs with quarter-wave symmetry as well as with only half-wave symmetry are computed. In particular, the quarter-wave symmetric pulse patterns are defined to be odd functions with half-wave symmetry, and are thus characterized by the angles over the first quarter of the fundamental period. The switching angles for the half-wave symmetric OPPs are shown in Fig. 13.

In Fig. 16, the maximum of the junction temperatures during a fundamental period and for the range of considered displacement angles is shown at each modulation index for GCTs 1 and 2, and Diodes 5 and 9. As can be seen, the maximum allowed junction temperature is often exceeded, especially in the case of GCT 1, where it is exceed by up to $15 \,^{\circ}$ C. Relaxing quarter-wave symmetry to half-wave symmetry has nearly no benefit in this case, neither in terms of maximum junction temperature nor in terms of current distortions, see Fig. 17.

To lower the temperature, without imposing thermal constraints, two options are available. The first one is to reduce the rated current $I_{\rm R}$ of the converter system. To satisfy the junction temperature limits, the rated current needs to be reduced to $I_{\rm R} = 2090$ A, derating the converter by 13 %.

The second option is to reduce the (device) switching frequency $f_{\rm sw}$. By adopting pulse number d = 2, the switching frequency is reduced to $f_{\rm sw} = 100$ Hz, which meets the thermal limits. This is achieved, however, at the expense of excessive current distortions, as can be seen in Fig. 17. In this case, relaxing quarter-wave symmetry to half-wave symmetry does have a tangible benefit. When reducing the pulse number from d = 3 to 2, the TDD increase is quite excessive. In particular, the current TDD averaged over the range of modulation indices from 0.85 to 1.23—the average current TDD—increases from 8.18 % to 12.49 % (i.e., by 53 %) for the half-wave symmetric OPPs. Even worse, the relative peak TDD increases from 10.12 % to 17.38 % (i.e., by 71 %).



Fig. 16: Maximum junction temperatures for OPPs with d = 3 but without thermal constraints. Results for OPPs with quarter-wave symmetry (dashed line) as well as with only half-wave symmetry (solid line) are shown.

C. OPPs with Thermal Constraints

OPPs with an upper-bounded junction temperature are now considered. To account for small model inaccuracies, the peak



Fig. 17: Current TDD for OPPs with d = 2 and 3 but without thermal constraints. Results for OPPs with quarter-wave symmetry (dashed lines) as well as with only half-wave symmetry (solid lines) are shown.

temperature is upper bounded at $T_{\text{lim}} = T_{\text{j,max}} - 2 \,^{\circ}\text{C}$. Consider pulse number d = 3 with the device switching frequency $f_{\text{sw}} = 150 \,\text{Hz}$. The switching angles for the halfwave symmetric OPP are shown in Fig. 18. As before, the maximum of the junction temperatures during a fundamental period and for the range of considered displacement angles is shown in Fig. 19. The junction temperature is always within the thermal limits of the devices, regardless of the symmetry imposed.

Imposing thermal constraints clearly increases the current TDD, since the additional constraints reduces the feasible region. This can be seen in Fig. 20, in which the current TDD of the thermally-constrained OPPs with d = 3 are compared with those of the traditional (thermally-unconstrained) OPPs. When using thermally-constrained quarter-wave symmetric OPPs, the TDD increases by a relative average of 13% compared to the traditional half-wave symmetric OPPs with d = 3. Furthermore, the peak TDD increases by 33%. However, by adopting half-wave symmetry for the thermal-constrained OPPs, the relative average TDD increase is reduced to 7%. The relative peak TDD increases by only 1%. Even though the benefit of relaxing quarter-wave symmetry to half-wave symmetry was minor in terms of current distortions for the traditional OPPs for the considered range of modulation indices, the thermally-constrained half-wave symmetric OPPs offer significantly lower harmonic distortions (especially regarding the peak TDD) compared to their quarter-wave symmetric counterparts.

D. Summary

In summary, compared to the traditional trial-and-error approach to limit the peak junction temperature, either by reducing the switching frequency or by lowering the rated current, the proposed method to formulate and impose constraints on the junction temperatures provides a significant performance boost in terms of current distortions and achievable rated current. This performance improvement is visualized in Fig. 21. The x-axis depicts the maximum violation of



Fig. 18: Switching angles of the half-wave symmetric OPP with d = 3 and with thermal constraints.

the semiconductor-specific thermal limit $T_{j,max}^{j}$ for the 10 semiconductor devices, i.e.,

$$T_{j,viol} = \max_{j \in \{1,2,...,10\}} (T_j^j - T_{j,max}^j).$$

We refer to this as the maximum junction temperature violation. Positive violations imply that at least one semiconductor violates its thermal limit, requiring derating of the current or operation at a lower switching frequency. The y-axis in Fig. 21 shows the current TDD averaged over the range of considered modulation indices ($0.85 \le m \le 1.23$), the average current TDD.

For traditional OPPs without thermal constraints, the device switching frequency had to be reduced from $f_{sw} = 150 \, \text{Hz}$ (d = 3) to 100 Hz (d = 2) to meet the thermal limits. This, in turn, increased the average current TDD from 8.18%to 12.49%, i.e., by 53%. The peak TDD increased from 10.12% to 17.38%, i.e., by 71%. Alternatively, if the switching frequency was to be kept at $f_{sw} = 150 \,\text{Hz}$, the rated current had to be reduced by 13%. Instead, when imposing the proposed thermal constraints when computing the OPP with pulse number d = 3, the peak junction temperature was reduced by 15 °C to meet the thermal limit, without any converter derating; the average current TDD increased from 8.18% to 8.74%, i.e., by only 7% relatively. Furthermore, the peak TDD only increased from 10.16% to 10.26%, i.e., by only 1% (relatively). In summary, computing thermallyconstrained OPPs-under the assumption that the semiconductors have been accurately parameterized-results in superior current TDDs when compared to traditional methods and avoids derating of the converter.

VII. CONCLUSIONS

In this paper, a thermal modeling framework to predict the junction temperatures of semiconductors was developed and verified. The method was tailored towards the computation of OPPs so that it could be included in the underlying numerical optimization problem. This enabled the computation of OPPs that resulted in constrained semiconductor junction temperatures, guaranteeing the operation of the semiconductor devices within their safe thermal operating area. The main



Fig. 19: Maximum junction temperatures for OPPs with d = 3 and with thermal constraints. Results for OPPs with quarter-wave symmetry (dashed line) as well as with only half-wave symmetry (solid line) are shown.

computational steps of this methodology are summarized in Fig. 22.

The proposed method offers an elegant way to maximize the



Fig. 20: Current TDD for OPPs with d = 3 and with thermal constraints. Results for OPPs with quarter-wave symmetry (dashed lines) as well as with only half-wave symmetry (solid lines) are shown. The thermally-constrained OPPs are also compared with half-wave symmetric OPPs with pulse numbers d = 2 and 3 but without thermal constraints (dash-dotted lines).



Fig. 21: Average current TDD versus maximum junction temperature violation $T_{j,viol}$ for the considered OPPs, either with thermal constraints (blue) or without (red). Results for OPPs with quarter-wave symmetry (squares) as well as with only half-wave symmetry (circles) are shown.

utilization of the semiconductors in terms of their switching and thermal capabilities while achieving the lowest possible harmonic current distortions. The possible optimization criteria are widespread. Instead of constraining the peak junction temperature, one might lower the average junction temperature or the temperature ripple. One might also limit or minimize the average switching (and conduction) losses of all semiconductor devices, see (24) and (44), with the aim to maximize the converter efficiency of the converter.

APPENDIX

Thanks to the thermal model being linear (by assuming temperature-independent losses), the temperature of a semiconductor device can be decomposed into its conduction and switching loss components as

$$\boldsymbol{T}(\theta,\phi) = \boldsymbol{T}_{\rm sw}(\theta,\phi) + \boldsymbol{T}_{\rm cond}(\theta,\phi), \tag{61}$$

where

$$\boldsymbol{T}_{sw}(\theta,\phi) = \boldsymbol{e}^{\boldsymbol{F}\theta}\boldsymbol{T}_{sw}(0,\phi) + \int_{0}^{\theta} \boldsymbol{e}^{\boldsymbol{F}(\theta-\vartheta)}\boldsymbol{G}p_{sw}(\vartheta,\phi) \, \mathrm{d}\vartheta$$
(62a)

$$\boldsymbol{T}_{\text{cond}}(\theta,\phi) = \boldsymbol{e}^{\boldsymbol{F}\theta}\boldsymbol{T}_{\text{cond}}(0,\phi) + \int_{0}^{\sigma} \boldsymbol{e}^{\boldsymbol{F}(\theta-\vartheta)}\boldsymbol{G}p_{\text{cond}}(\vartheta,\phi) \,\,\mathrm{d}\vartheta.$$
(62b)

A. Switching Loss Component

First, consider the switching loss component. Recall from (22) that

$$p_{\rm sw}(\theta,\phi) = \omega_1 \frac{v_{\rm dc}}{2} \sum_{i=1}^{4d} c_i z(\theta,\phi) \delta(\theta - \alpha_i)$$

Using the sifting property of the impulse

$$\int_{-\infty}^{x} f(x)\delta(x-a)dx = f(a)h(x-a),$$

the integral of (62a) can easily be solved, resulting in

$$\boldsymbol{T}_{sw}(\theta,\phi) = \boldsymbol{e}^{\boldsymbol{F}\theta}\boldsymbol{T}_{sw}(0,\phi) + \omega_1 \frac{v_{dc}}{2} \sum_{i=1}^{4d} \boldsymbol{e}^{\boldsymbol{F}(\theta-\alpha_i)} c_i z(\alpha_i,\phi) h(\theta-\alpha_i) \boldsymbol{G}.$$
(63)

Then, with $\theta = 2\pi$, $T_{sw}(0, \phi) =$

$$\begin{aligned} 0,\phi) &= \boldsymbol{e}^{\boldsymbol{F}2\pi}\boldsymbol{T}_{\mathrm{sw}}(0,\phi) \\ &+ \omega_1 \frac{v_{\mathrm{dc}}}{2} \sum_{i=1}^{4d} \boldsymbol{e}^{\boldsymbol{F}(2\pi-\alpha_i)} c_i \boldsymbol{z}(\alpha_i,\phi) \boldsymbol{G}, \end{aligned}$$

where the fact was used that $T_{sw}(0, \phi) = T_{sw}(2\pi, \phi)$ needs to hold during steady-state operation. The initial value can then be calculated as

$$\boldsymbol{T}_{\rm sw}(0,\phi) = (\mathbf{I}_n - \boldsymbol{e}^{\boldsymbol{F}2\pi})^{-1} \omega_1 \frac{v_{\rm dc}}{2} \sum_{i=1}^{4d} \boldsymbol{e}^{\boldsymbol{F}(2\pi - \alpha_i)} c_i z(\alpha_i,\phi) \boldsymbol{G}.$$
(64)

After inserting (64) into (63), the temperature due to the switching loss component can be calculated at any angle θ .

B. Conduction Loss Component

Next, consider the conduction loss component. Recall from (43) that the conduction losses are

$$p_{\rm cond}(\theta,\phi) = \sqrt{2}V_{\rm on}I\nu(\theta,\phi) + b2R_{\rm on}(I)^2\mu(\theta,\phi), \quad (65)$$

where

$$\nu(\theta,\phi) = \sum_{i=0}^{12d+2} \Delta \bar{s}_i h(\theta - \bar{\alpha}_i) \sin(\theta + \phi)$$
$$\mu(\theta,\phi) = \frac{1}{2} \sum_{i=0}^{12d+2} \Delta \bar{s}_i h(\theta - \bar{\alpha}_i) (1 - \cos(2(\theta + \phi))).$$

For the term $\mu(\theta, \phi)$ we used the fact that $(\sin(\theta + \phi))^2 = \frac{1}{2}(1 - \cos(2(\theta + \phi)))$ holds. Inserting (65) into (62b) results in

$$T_{\text{cond}}(\theta, \phi) = e^{F\theta} T_{\text{cond}}(0, \phi) + \sqrt{2V_{\text{on}}I}\eta(\theta, \phi) + bR_{\text{on}}(I)^2(\rho(\theta, \phi) - \kappa(\theta, \phi))$$
(66)



Fig. 22: Computational steps to derive the junction temperatures so that they can be constrained in the OPP optimization problem.

with

$$\boldsymbol{\eta}(\theta,\phi) = \sum_{i=0}^{12d+2} \Delta \bar{s}_i \int_{\bar{\alpha}_i}^{\theta} \boldsymbol{e}^{\boldsymbol{F}(\theta-\vartheta)} \sin(\vartheta+\phi) \mathrm{d}\vartheta \boldsymbol{G} h(\theta-\bar{\alpha}_i)$$
(67a)

$$\boldsymbol{\kappa}(\theta,\phi) = \sum_{i=0}^{12d+2} \Delta \bar{s}_i \int_{\bar{\alpha}_i}^{\theta} \boldsymbol{e}^{\boldsymbol{F}(\theta-\vartheta)} \cos(2(\vartheta+\phi)) \mathrm{d}\vartheta \boldsymbol{G}h(\theta-\bar{\alpha}_i)$$
(67b)

$$\boldsymbol{\rho}(\theta) = \sum_{i=0}^{12d+2} \Delta \bar{s}_i \int_{\bar{\alpha}_i}^{\theta} \boldsymbol{e}^{\boldsymbol{F}(\theta-\vartheta)} \mathrm{d}\vartheta \, \boldsymbol{G}h(\theta-\bar{\alpha}_i). \tag{67c}$$

Here, we used the fact that a step function changes the lower bound of an integral as

$$\int_{-\infty}^{x} f(x)h(x-a) \, \mathrm{d}x = \int_{a}^{x} f(x) \, \mathrm{d}xh(x-a).$$

The integrals of (67a) and (67b) can be solved via integration by parts, whereas (67c) is straightforward to integrate:

$$\boldsymbol{\eta}(\theta,\phi) = \sum_{i=0}^{12d+2} \Delta \bar{s}_i \boldsymbol{e}^{\boldsymbol{F}\theta} \left(\boldsymbol{M}(\theta,\phi) - \boldsymbol{M}(\bar{\alpha}_i,\phi) \right) \boldsymbol{G}h(\theta - \bar{\alpha}_i)$$
(68a)

$$\boldsymbol{\kappa}(\theta,\phi) = \sum_{i=0}^{12d+2} \Delta \bar{s}_i \boldsymbol{e}^{\boldsymbol{F}\theta} \left(\boldsymbol{N}(\theta,\phi) - \boldsymbol{N}(\bar{\alpha}_i,\phi) \right) \boldsymbol{G}h(\theta - \bar{\alpha}_i)$$
(68b)

$$\boldsymbol{\rho}(\theta) = \boldsymbol{F}^{-1} \sum_{i=0}^{12d+2} \Delta \bar{s}_i \left(\boldsymbol{e}^{\boldsymbol{F}(\theta - \bar{\alpha}_i)} - \mathbf{I}_n \right) \boldsymbol{G} h(\theta - \bar{\alpha}_i),$$
(68c)

where

$$M(\vartheta, \phi) = -(\mathbf{I}_n + \mathbf{F}^2)^{-1} e^{-\mathbf{F}\vartheta} (\mathbf{F} \sin(\vartheta + \phi) + \mathbf{I}_n \cos(\vartheta + \phi))$$
$$N(\vartheta, \phi) = (4\mathbf{I}_n + \mathbf{F}^2)^{-1} e^{-\mathbf{F}\vartheta} (2\mathbf{I}_n \sin(2(\vartheta + \phi)) - \mathbf{F} \cos(2(\vartheta + \phi))).$$

With $\theta = 2\pi$, and using the fact that $T_{\text{cond}}(0, \phi) = T_{\text{cond}}(2\pi, \phi)$ holds at steady-state, (66) yields the initial value

$$\boldsymbol{T}_{\text{cond}}(0,\phi) = (\mathbf{I}_n - \boldsymbol{e}^{\boldsymbol{F}2\pi})^{-1} \left(V_{\text{on}} \sqrt{2} I \boldsymbol{\eta}(2\pi,\phi) + b(I)^2 R_{\text{on}}(\boldsymbol{\rho}(2\pi,\phi) - \boldsymbol{\kappa}(2\pi,\phi)) \right).$$
(69)

After inserting (69) into (66), the temperature due to the conduction loss component can be calculated at any angle θ .

Here, any functions that may cause discontinuities in the gradients can easily be approximated by a smooth function. For example, the hyperbolic tangent function of (15) can be used to approximate a step function.

REFERENCES

- G. S. Buja and G. B. Indri, "Optimal pulsewidth modulation for feeding AC motors," *IEEE Transactions on Industry Applications*, vol. IA-13, pp. 38–44, Jan. 1977.
- [2] G. S. Buja, "Optimum output waveforms in PWM inverters," *IEEE Transactions on Industry Applications*, vol. IA-16, pp. 830–836, Nov. 1980.
- [3] A. K. Rathore, J. Holtz, and T. Boller, "Synchronous optimal pulsewidth modulation for low-switching-frequency control of medium-voltage multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, pp. 2374–2381, July 2010.
- [4] A. K. Rathore, J. Holtz, and T. Boller, "Generalized optimal pulsewidth modulation of multilevel inverters for low-switching-frequency control of medium-voltage high-power industrial AC drives," *IEEE Transactions* on Industrial Electronics, vol. 60, pp. 4215–4224, Oct. 2013.
- [5] J. Scoltock, T. Geyer, and U. K. Madawala, "A comparison of model predictive control schemes for MV induction motor drives," *IEEE Transactions on Industrial Informatics*, vol. 9, pp. 909–919, May 2013.

- [6] P. Steimer, H. Gruning, J. Werninger, E. Carroll, S. Klaka, and S. Linder, "IGCT—a new emerging technology for high power, low cost inverters," *IEEE Industry Applications Magazine*, vol. 5, no. 4, pp. 12–18, 1999.
- [7] P. Steimer, O. Apeldoorn, E. Carroll, and A. Nagel, "IGCT technology baseline and future opportunities," in 2001 IEEE/PES Transmission and Distribution Conference and Exposition, vol. 2, (Atlanta, GA, USA), pp. 1182–1187, 2001.
- [8] J. Nelson, G. Venkataramanan, and A. El-Refaie, "Fast thermal profiling of power semiconductor devices using Fourier techniques," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 2, pp. 521–529, 2006.
- [9] J. Shen, S. Schroder, H. Stagge, and R. W. De Doncker, "A fast and precise simulation method for performance screening for high power converter designs," in 2012 IEEE Energy Conversion Congress and Exposition (ECCE), (Raleigh, NC, USA), pp. 4418–4425, IEEE, Sept. 2012.
- [10] M. Andresen, K. Ma, G. Buticchi, J. Falck, F. Blaabjerg, and M. Liserre, "Junction temperature control for more reliable power electronics," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 765–776, 2018.
- [11] J. Kuprat, C. H. van der Broeck, M. Andresen, S. Kalker, M. Liserre, and R. W. De Doncker, "Research on active thermal control: actual status and future trends," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 6, pp. 6494–6506, 2021.
- [12] T. Geyer, Model predictive control of high power converters and industrial drives. Chichester, UK: John Wiley & Sons, Ltd, Nov. 2016.
- [13] A. Birth, T. Geyer, H. d. T. Mouton, and M. Dorfling, "Generalized three-level optimal pulse patterns with lower harmonic distortion," *IEEE Transactions on Power Electronics*, vol. 35, pp. 5741–5752, June 2020.
- [14] Infineon, "Transient thermal measurements and thermal equivalent circuit models, AN2015-10." Online document: https://www.infineon.com.
- [15] H. Energy, "Asymmetric Integrated Gate-Commutated Thyristor 5SHY 55L4500." Online document: https://www.hitachienergy.com/productsand-solutions/semiconductors/.
- [16] H. Energy, "Fast Recovery Diode 5SDF 20L4520." Online document: https://www.hitachienergy.com/products-and-solutions/semiconductors/.