On Bounding the Junction Temperature by Means of Optimal Modulation with Relaxed Properties

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***Abstract*—This paper presents the computation of three-level optimized pulse patterns (OPPs) that can keep the junction temperature bounded. Adding a thermal constraint, however, compromises the output current quality. To tackle this issue, OPPs with relaxed symmetry properties and multipolar switch positions are allowed. As a result, the harmonics remain low and close to those of conventional OPPs, as demonstrated by the presented results. Nevertheless, by relaxing the OPP properties, the computation time increases drastically. To exploit the benefits of the proposed OPPs, an efficient computation method is developed to keep the computation time modest. This is done by employing the concept of virtual switching angles that encapsulate the OPP switching transitions and the switching angles.**

***Index Terms*—Optimal modulation, pulse width modulation (PWM), multilevel converters, power losses, thermal stress, reliability**

I. Introduction

The semiconductor devices are the most expensive and vulnerable components in high-power electronics. To ensure operation within their safe operating area, the maximum junction temperature limit defined by the manufacturers should always be respected. By guaranteeing safe and reliable operation close to the thermal limits, the instantaneous converter capability can be fully utilized [1].

Since the switching losses have a direct effect on the junction temperature, it is common practice to manipulate them by means of control and modulation. With regards to the former, the control problem can be designed such that the thermal stress is either indirectly or directly addressed. For example, [2] reduces the switching losses by simultaneously decreasing the switching frequency and the output current. More versatile control techniques, such as model predictive control (MPC), can be designed to account for the thermal stress in the objective function of the MPC problem [3]. This equips the control scheme with degrees of freedom that enable the adjustment of the trade-off between current harmonic distortions and thermal performance [4].

As for modulation techniques, the losses can be decreased by either reducing the switching frequency or applying some form of discontinuous pulse width modulation (PWM) [5]. For example, by altering the discontinuous PWM pattern different thermal performance can be achieved [6]. Moreover, discontinuous PWM can be modified to keep the switching losses below a specific bound [7]. With all aforementioned options, however, the output current quality deteriorates when the number of pulses per fundamental period decreases. To improve the trade-off between output current quality and reliability, [8] proposes to employ discontinuous PWM only when the devices reach a critical end-of-life threshold. An alternative approach to improving the said trade-off is to choose the switching frequency by assessing the ratio between the expected lifetime extension and current total harmonic distortion (THD) deterioration [9].

However, when high-power applications are of interest, as in this work, the aforementioned trade-off produced with the discussed methods can be particularly poor. To achieve a favorable compromise between current quality and thermal stress, optimized pulse patterns (OPPs) can be considered, since they achieve low harmonic distortions at low switching frequencies [10]. Moreover, the switching losses produced by OPPs can be further reduced by accounting for them in the OPP optimization problem. In this direction, [11] modified the OPP problem to keep the switching power losses bounded while still producing currents of high quality. To facilitate such a favorable trade-off between losses and current quality, [11] adopted the OPP symmetry relaxations proposed in [12]. In doing so, the search space of the optimization problem increased, thus allowing for more degrees of freedom during the OPP computation process. By exploiting this feature, the robustness of such loss-bounded OPPs to changes in the power factor can also be improved [13].

Nevertheless, the switching losses are merely a proxy of the junction temperature. Therefore, to successfully address potential issues linked to the junction temperature, it is beneficial to formulate the OPP problem to directly account for it. For this reason, the computation of OPPs with explicit bounds on the temperature was proposed in [14]. Similarly to [11], that work proposed OPPs with relaxed, i.e., half-wave, symmetry to improve the trade-off between the junction temperature and the total demand distortion (TDD) of the output current.

Motivated by [14], this paper extends this concept by allowing multipolar switching sequences to effectively relieve the most thermally stressed devices. As shown in [12], such sequences can have a positive impact on the performance of OPPs. However, allowing for multipolar switching sequences

results in an exponential increase in the number of candidate sequences as the pulse number increases. Hence, exhaustively enumerating all available sequences and solving an optimization problem for each one of them would significantly increase the computational time. To tackle this issue, the proposed OPP problem is reformulated such that it returns the optimal switching sequence without iterating over all candidate options, thus significantly alleviating the required computational time. To do so, the concept of virtual angles—initially presented in [15]—is adopted to combine the information of switching angles and transitions in one optimization variable. The presented numerical results based on a three-level neutral-point-clamped (NPC) converter demonstrate the benefits of the proposed approach both in terms of the junction temperature–current TDD trade-off as well as required computation time.

II. Conventional Three-Level OPPs

Let the ratio between the device switching frequency f_{sw} and the fundamental frequency f_1 be the pulse number d, i.e., $d = \frac{f_{\text{sw}}}{f_1}$. A 2π-periodic three-level switching signal $u(\theta)$ is characterized by $4d+1$ switch positions $u_j \in \{-1, 0, 1\}$, $j \in \{0, \ldots, 4d\}$, and $4d$ switching angles α_i, $i \in \{1, \ldots, 4d\}$, at which a switching transition $\Delta u_i = u_i - u_{i-1} \in \{-1, 1\}$ occurs. To compute the signal $u(\theta)$, i.e., the $4d+1$ switch positions and $4d$ switching angles of the OPP, that results in the minimum current distortions, an objective function that captures the load current TDD I_{TDD} is formulated. Note that the latter is proportional to the weighted sum of the switching harmonics $\hat{u}_n = \sqrt{a_n^2 + b_n^2}$ when an inductive load is assumed, where a_n and b_n are the Fourier coefficients of the n^{th} OPP harmonic. For an analytical derivation of the current TDD expression as well as the a_n and b_n Fourier coefficients, the reader is referred to [12].

Conventional OPPs assume three-phase symmetry, quarter- and half-wave symmetry (QaHWS), and unipolar switching. Therefore, they can be fully described with only d switching angles $\boldsymbol{\alpha} \equiv \boldsymbol{\alpha}_Q = [\alpha_1 \ \alpha_2 \ \ldots \ \alpha_d]^T \in [0, \pi/2]^d$, while the switch positions are deterministic. Consequently, the optimization problem to compute such OPPs is

$$\begin{aligned} \underset{\boldsymbol{\alpha}_Q}{\text{minimize}} \quad & J_1(\boldsymbol{\alpha}_Q) = \textstyle\sum_{n=5,7,\ldots} \left(\frac{b_n}{n}\right)^2 \\ \text{subject to} \quad & b_1 = m \\ & 0 \le \alpha_1 < \alpha_2 < \ldots < \alpha_d \le \tfrac{\pi}{2}\,, \end{aligned} \tag{1}$$

where $m \in [0, 4/\pi]$ is the desired modulation index. Note that the a_n Fourier coefficients and even harmonics are zero due to the QaHWS, while triplen harmonics do not drive harmonic current when a load in wye configuration with a floating star point is assumed.

III. Thermally-Constrained Three-Level OPPs

A. Junction Temperature Calculation for an NPC Converter

A three-level NPC converter with a machine is shown in Fig. 1. In each phase, there are four active switches S_1 to S_4 with their respective freewheeling diodes D_1 to D_4, and

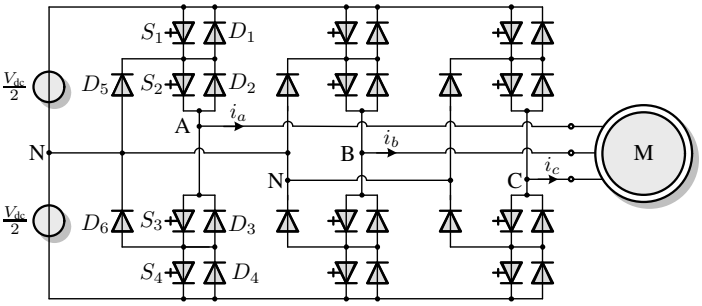


Fig. 1: Three-level neutral-point-clamped (NPC) converter driving a machine.

TABLE I: Semiconductor device parameters

GCT 5SHY 55L4500		
Turn-on losses	e_{on}	1.8 J
Turn-off losses	e_{off}	26.5 J
GCT coefficient	a_{GCT}	1.12 V
GCT coefficient	b_{GCT}	$0.26 \cdot 10^{-3}$ V/A
Max. junction temp.	$T_{\text{j,max}}$	125°C
Thermal resistances	R_{1-6}	5.56, 1.53, 0.87, 0.55, 7.0, 2.4 K/kW
Time constants	τ_{1-6}	512, 89.6, 9.1, 2.4, 9000, 3000 ms
Diode 5SDF 20L4520		
Reverse recov. losses	e_{rr}	13.9 J
Diode coefficient	a_{diode}	1.7 V
Diode coefficient	b_{diode}	$0.8 \cdot 10^{-3}$ V/A
Max. junction temp.	$T_{\text{j,max}}$	135°C
Thermal resistances	R_{1-6}	3.71, 1.43, 0.69, 0.18, 2.5, 10.4 K/kW
Time constants	τ_{1-6}	534, 67.0, 7.4, 1.1, 4000, 8000 ms

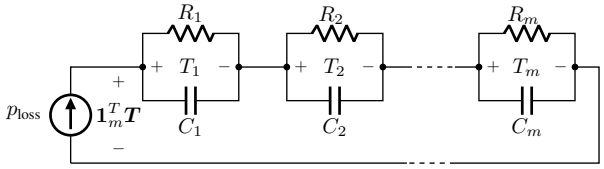


Fig. 2: Foster model of the m^{th} order.

two clamping diodes D_5 and D_6. In this work, the semiconductor devices used are the 5SHY 55L4500 integrated-gate-commutated thyristor (IGCT) [16] and the 5SDF 20L4520 diode [17]. The parameters of the semiconductor devices at rated maximum values of anode-cathode voltage $v_T = 2.8\,\text{kV}$ and anode current $i_T = 4\,\text{kA}$ are given in Table I.

For the computation of the semiconductor junction temperature, the m^{th}-order Foster model is used, see Fig. 2. It consists of m RC-networks that model the heat transfer from the junction through the case to the cooling water. Considering the frequency domain, the junction temperature is given by

$$T_{\text{j}}(s) = P_{\text{loss}}(s) \cdot Z_{\text{th}}(s) + T_{\text{w}}\,, \tag{2}$$

where T_{w} is the temperature of the cooling water and

$$Z_{\text{th}}(s) = \sum_{i=1}^{m} \frac{R_i}{\tau_i s + 1} \tag{3}$$

is the transient thermal resistance with time constant $\tau_i = R_i C_i$.

TABLE II: Switching energy losses in an NPC phase leg.

Polarity of phase current i_x	Switching transition	Switching energy losses
>0	$0 \to 1$	$e_{\text{on},S_1} + e_{\text{rr},D_5}$
	$1 \to 0$	e_{off,S_1}
	$0 \to -1$	e_{off,S_2}
	$-1 \to 0$	$e_{\text{on},S_2} + e_{\text{rr},D_4}$
<0	$0 \to 1$	e_{off,S_3}
	$1 \to 0$	$e_{\text{on},S_3} + e_{\text{rr},D_1}$
	$0 \to -1$	$e_{\text{on},S_4} + e_{\text{rr},D_6}$
	$-1 \to 0$	e_{off,S_4}

TABLE III: Conduction energy losses in an NPC phase leg.

Polarity of phase current i_x	Switch position	Conduction energy losses
>0	1	$e_{\text{con},S_1} + e_{\text{con},S_2}$
	0	$e_{\text{con},S_2} + e_{\text{con},D_5}$
	-1	$e_{\text{con},D_3} + e_{\text{con},D_4}$
<0	1	$e_{\text{con},D_1} + e_{\text{con},D_2}$
	0	$e_{\text{con},S_3} + e_{\text{con},D_6}$
	-1	$e_{\text{con},S_3} + e_{\text{con},S_4}$

In the time domain, the junction temperature T_j can be computed with the following system of differential equations

$$\frac{\mathrm{d}\boldsymbol{T}(\theta)}{\mathrm{d}\theta} = \boldsymbol{F}\boldsymbol{T}(\theta) + \boldsymbol{G}p_\text{loss}(\theta) \tag{4a}$$

$$T_\text{j}(\theta) = \mathbf{1}_n^T\boldsymbol{T}(\theta) + T_\text{w}\,, \tag{4b}$$

where $p_\text{loss}(\theta)$ are the instantaneous losses at angle θ, $\boldsymbol{T} = [T_1\ T_2\ \dots\ T_m]^T$ is the vector of temperatures T_k of the RC-networks, with $k = 1, 2, \dots, m$, and $\mathbf{1}_m$ is a vector of ones. Finally, the system matrix $\boldsymbol{F}$ and output vector $\boldsymbol{G}$ are

$$\boldsymbol{F} = \begin{bmatrix} -\frac{1}{\tau_1} & 0 & \dots & 0 \\ 0 & -\frac{1}{\tau_2} & & \vdots \\ \vdots & & \ddots & \vdots \\ 0 & 0 & \dots & -\frac{1}{\tau_m} \end{bmatrix} \frac{1}{\omega_1}, \text{ and } \boldsymbol{G} = \begin{bmatrix} \frac{1}{C_1} \\ \frac{1}{C_2} \\ \vdots \\ \frac{1}{C_m} \end{bmatrix} \frac{1}{\omega_1},$$

where ω_1 is the fundamental angular frequency.

As shown in [14], the instantaneous value of the temperatures at angle θ can be found by integrating (4a), yielding

$$\boldsymbol{T}(\theta) = \boldsymbol{e}^{\boldsymbol{F}\theta}\boldsymbol{T}(0) + \int_0^\theta \boldsymbol{e}^{\boldsymbol{F}(\theta-x)}\boldsymbol{G}p_\text{loss}(x)\,\mathrm{d}x\,, \tag{5}$$

where $\boldsymbol{e}$ is the matrix exponential, while the initial temperature $\boldsymbol{T}(0)$ is given by

$$\boldsymbol{T}(0) = \left(\boldsymbol{I}_m - \boldsymbol{e}^{\boldsymbol{F}2\pi}\right)^{-1} \int_0^{2\pi} \boldsymbol{e}^{\boldsymbol{F}(\theta-x)}\boldsymbol{G}p_\text{loss}(x)\,\mathrm{d}x\,,$$

due to the 2π-periodicity of the applied OPP. Therefore, as it can be deduced from (5), the instantaneous losses are required for the calculation of the junction temperature. Due to the OPP symmetries, it suffices to compute p_loss in only one phase leg of the NPC converter. To do so, the devices that turn on and off at each OPP switching event in the phase leg are identified based on the polarity of the commutated current. The latter is considered sinusoidal with frequency f_1, i.e., $i(t) = I\sin(2\pi f_1 t - \phi)$, where I is the amplitude of the current and ϕ the angular displacement between the phase current and voltage. Subsequently, the incurred losses are computed based on the instantaneous value of the current and the dc-link voltage, which is assumed to be constant. The instantaneous switching and conduction losses are summarized in Tables II and III, respectively, where e_on/e_off denote the turn-on/off energy losses of the IGCTs, e_rr the reverse recovery energy losses of the diodes, and e_con the conduction energy losses.[1]

Hence, based on the above, it can be concluded that the junction temperature T_j of each device at switching angle α_i can be computed using (5) and (4b) with $\theta = \alpha_i$. As can be seen, this temperature is a function of the applied OPP, phase current, and displacement angle ϕ. Therefore, as shown in [14], it can be computed in the OPP optimization procedure, and consequently directly manipulated during this process, as explained in the sequel of this section.

B. Symmetry-Relaxed OPP Problem to Limit the Junction Temperature

To account for the junction temperature in the OPP computation the maximum junction temperature of all devices is bounded by adding the constraint[2]

$$T^\ell_{\text{j},\max}(\boldsymbol{\alpha}, \phi) \leq T^\ell_{\text{j,lmt}}\ \forall \ell \in \{S_{1,2}, D_{1,2,5}\}\,, \tag{6}$$

to the optimization problem (1), where $T^\ell_{\text{j,lmt}}$ is 125°C and 135°C for the IGCTs and diodes, respectively, used in this work. It should be pointed out that, due to the high switching losses of the selected devices, the maximum junction temperature most probably occurs after a switching transition. Therefore the maximum junction temperature $T^\ell_{\text{j},\max}$ of each device is assumed to be

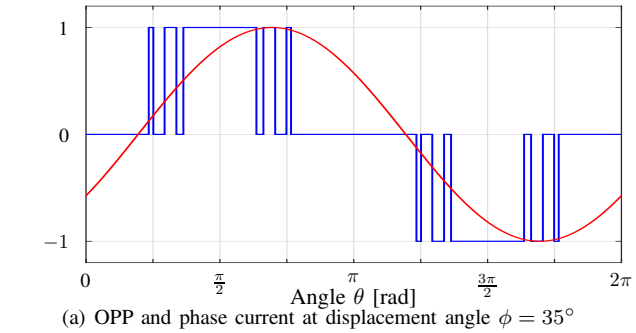
$$T^\ell_{\text{j},\max} = \max\{T^\ell_\text{j}(\alpha_i)\}\,, i \in \{1, \dots, 4d\}\,, \tag{7}$$

and it is a function of the applied OPP, phase current, and displacement angle ϕ.

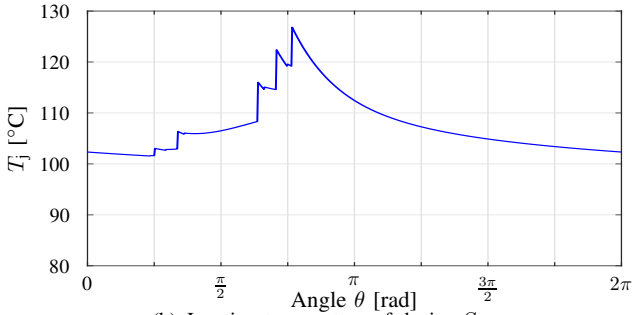
OPPs that are computed based on the revised OPP problem—i.e., problem (1) with constraint (6)—can guarantee that the junction temperature remains within the desired limits. Nevertheless, in doing so, the quality of the current TDD is compromised as a trade-off between T_j and I_TDD arises. As recently shown in [14], this trade-off can be improved by relaxing the symmetry of the OPP and allowing for half-wave symmetry (HWS). This relaxation increases the search space of the three-level OPP problem since the OPP switching angles can be more freely distributed over the half-period. As a result, the increased harmonic distortions caused by additional

[1]The detailed computation of the losses is provided in [11] and [13].

[2]Due to the single- and three-phase symmetry properties of OPPs, the devices in the pairs $\{S_1, S_4\}$, $\{D_1, D_4\}$, $\{S_2, S_3\}$, $\{D_2, D_3\}$, and $\{D_5, D_6\}$ have the same losses, see also [11]. Hence, it suffices to constraint the junction temperature of the five semiconductor devices in the upper half of one NPC leg, namely S_1, S_2, D_1, D_2, and D_5.

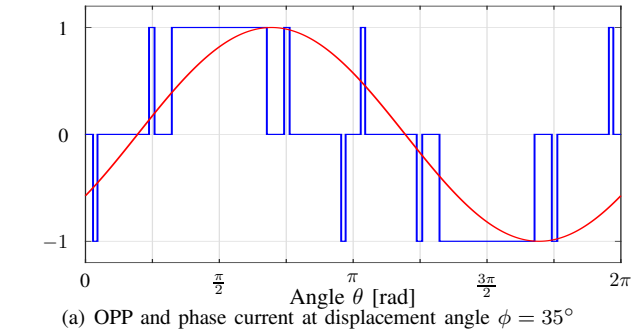


(a) OPP and phase current at displacement angle $\phi = 35°$

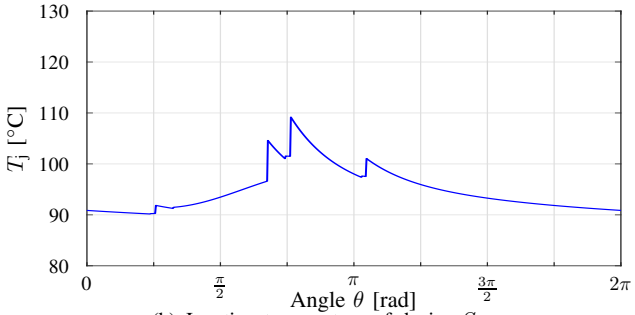


(b) Junction temperature of device S_1

Fig. 3: Unipolar QaHWS OPP with $d = 5$ at modulation index $m = 0.72$



(a) OPP and phase current at displacement angle $\phi = 35°$



(b) Junction temperature of device S_1

Fig. 4: Multipolar HWS OPP with $d = 5$ at modulation index $m = 0.72$.

constraints in the optimization problem can be mitigated, thus enabling an improved I_{TDD}–T_{j} trade-off.

With the above relaxation, $2d$ switching angles $\boldsymbol{\alpha} \equiv \boldsymbol{\alpha}_H = [\alpha_1 \ \alpha_2 \ \dots \ \alpha_{2d}]^T \in [0, \pi]^{2d}$ are needed to fully describe $u(\theta)$. As a result, the optimization problem that accounts for the thermal constraints is revised to the following form [14]

$$\begin{aligned} \underset{\boldsymbol{\alpha}_H}{\text{minimize}} \quad & J(\boldsymbol{\alpha}_H) = \textstyle\sum_{n=5,7,11,\dots} \frac{a_n^2 + b_n^2}{n^2} \\ \text{subject to} \quad & a_1 = 0, \ b_1 = m \\ & 0 \leq \alpha_1 < \alpha_2 < \dots < \alpha_{2d} \leq \pi \\ & T^{\ell}_{\text{j,max}}(\boldsymbol{\alpha}_H, \phi) \leq T^{\ell}_{\text{j,lmt}} \, \forall \ell \in \{S_{1,2}, D_{1,2,5}\} \, . \end{aligned} \tag{8}$$

Note that, as with problem (1), only odd non-triplen harmonics are considered since even harmonics remain zero due to the HWS, while triplen harmonics do not affect the current. Moreover, $a_1 = 0$ such that the phase of the fundamental component is zero.

C. Thermally-Constrained Multipolar HWS OPPs

As demonstrated in [12], besides symmetry relaxations, relaxing the polarity of the OPP switch positions can have a beneficial impact on the output current quality. This means that the single-phase OPP can assume all possible values in the first half of the period, i.e., $u_j \in \{-1, 0, 1\}$, for $j \in \{0, 1, \dots, 2d\}$. In the context of thermally-constrained OPPs, multipolar switch positions can potentially have another advantage since the junction temperature of the devices that are predominantly used during half of the period has more time to drop, thus keeping the thermal stress at bay.

An example of the benefit of multipolar OPPs is shown in Figs. 3 and 4, for modulation index $m = 0.72$, displacement angle $\phi = 35°$, and rated current 2.8 kA. The said displacement angle and chosen operating conditions imply that devices S_1 and D_5 produce switching losses, while devices S_1, S_2 and D_5 produce conduction losses, see Tables II and III, respectively. Since the switching losses have a bigger impact on the junction temperature, and the IGCTs have higher switching losses than the diodes, it can be deduced that the most thermally stressed device is the outer switch S_1. For this reason, the junction temperature of this device is displayed in Figs. 3(b) and 4(b). As can be seen, when conventional (unipolar) OPPs are applied (see Fig. 3), the maximum steady-state junction temperature is $T_{\text{j,max}} = 127°\text{C}$. This temperature is above the IGCT safe operation limit of 125°C, meaning that this pattern could harm this device. To avoid this, the output current could be reduced, thus decreasing the output power of the converter. Alternatively, an OPP with a lower pulse number could be used instead, thus reducing the switching frequency at a cost of a higher current TDD. These problems can be avoided with multipolar HWS OPPs, see Fig. 4. Even though operation at the same switching frequency is assumed, the maximum junction temperature of switch S_1 is only $T_{\text{j,max}} = 109°\text{C}$. This is achieved thanks to the implemented negative switch positions that remove some of the switching losses from S_1 and distribute them among other devices, e.g., S_2 and S_4.

Given the above, thermally-constrained multipolar HWS OPPs are proposed in this work. To compute such OPPs, the $2d$ optimal switching angles $\boldsymbol{\alpha}_H$ and the $2d$ optimal switch positions $\boldsymbol{u}_H = [u_0 \ u_1 \ \dots \ u_{2d-1}]^T$ have to be found. This requires the evaluation of $2^{d+1} - 1$ possible sequences for a given pulse number d. Such an exponential increase in the number of candidate sequences, however, indicates a significant increase in the complexity of the—already difficult to solve—relaxed OPP problem, making the computation of

multipolar HWS OPPs a very challenging task.

This work overcomes this issue by solving the thermally-constrained multipolar HWS OPP problem only *once* per initial switch position $u_0 \in \{-1, 0, 1\}$. To do so, the switching angle $\alpha_i \in [0, \pi]$ and the switch transition $\Delta u_i \in \{-1, 1\}$ are combined into one optimization variable, as proposed in [15]. This new variable, referred to as virtual angle γ_i, is defined as

$$\gamma_i = \alpha_i + \frac{1 - \Delta u_i}{2}\pi \,. \tag{9}$$

As can be inferred from (9), in contrast to the switching angles α_i which assume values in $[0, \pi]$, the virtual angles γ_i assume values in $[0, 2\pi]$. Specifically, the virtual angles $\gamma_i \in [0, \pi]$ correspond to positive switching transitions $\Delta u_i = 1$ with $\gamma_i = \alpha_i$, meaning that

$$\sin(n\gamma_i) = \sin(n\alpha_i) = \Delta u_i \sin(n\alpha_i)\,,$$

and

$$\cos(n\gamma_i) = \cos(n\alpha_i) = \Delta u_i \cos(n\alpha_i)\,.$$

On the other hand, the virtual angles $\gamma_i \in [\pi, 2\pi]$ correspond to negative switching transitions $\Delta u_i = -1$ with $\gamma_i = \alpha_i + \pi$, resulting in

$$\begin{aligned}\sin(n\gamma_i) &= \sin(n(\alpha_i + \pi)) = \sin(n\alpha_i)\cos(n\pi) \\ &= -\sin(n\alpha_i) = \Delta u_i \sin(n\alpha_i)\ \forall n \text{ odd}\,,\end{aligned}$$

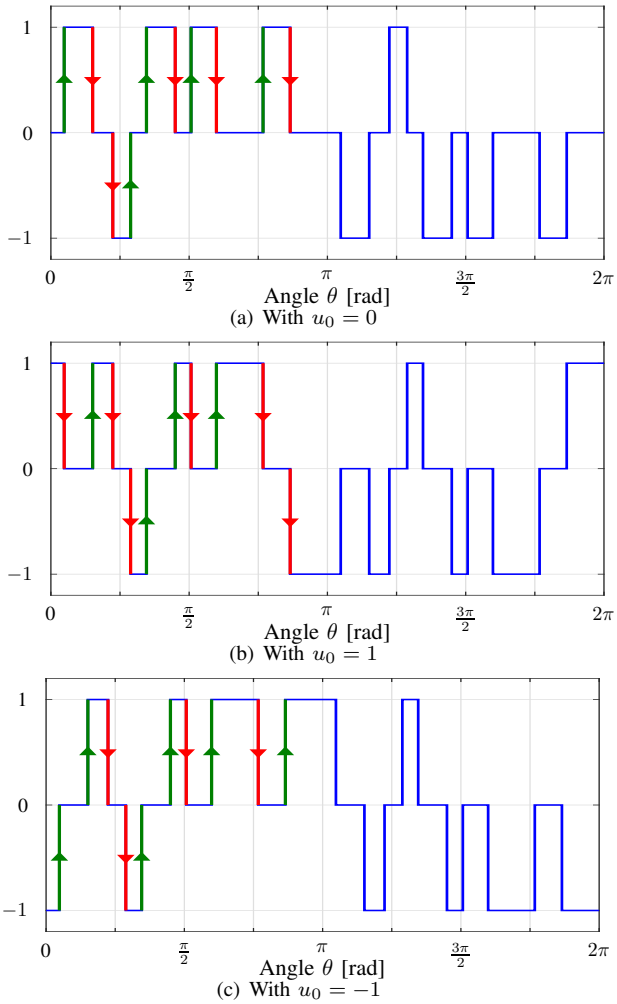
and

$$\begin{aligned}\cos(n\gamma_i) &= \cos(n(\alpha_i + \pi)) = \cos(n\alpha_i)\cos(n\pi) \\ &= -\cos(n\alpha_i) = \Delta u_i \cos(n\alpha_i)\ \forall n \text{ odd}\,.\end{aligned}$$

Hence, based on the above, the Fourier coefficients a_n and b_n can be written as a function of γ_i. This implies that the OPP objective function can be reformulated accordingly to account for this.

Following, the constraints on the virtual angles need to be defined. Taking into account that the value of γ_i determines the polarity of the switching transition, the number of positive and negative positive switching transitions has to be identified. This can be done by observing that the number of positive and negative OPP switching transitions depends on the initial switch position u_0, see Fig. 5. When $u_0 = 0$, d switching transitions are positive and d negative, highlighted with green and red arrows, respectively, in Fig. 5(a). In the case of $u_0 = 1$, $d - 1$ switching transitions are positive and $d + 1$ negative, see Fig. 5(b). Finally, $d + 1$ switching transitions are positive and $d - 1$ negative when $u_0 = 1$, see Fig. 5(c). Therefore, by combining all cases, $d - u_0$ virtual angles relate to positive switching transitions, meaning $\gamma_i \in [0, \pi]$ for $i \in \{1, \ldots, d - u_0\}$, while $d + u_0$ virtual angles relate to negative switching transitions, i.e., $\gamma_i \in [\pi, 2\pi]$ for $i \in \{d - u_0 + 1, \ldots, 2d\}$.

Finally, unlike conventional OPPs where the unipolar switch positions are deterministic, the multipolar switch positions of the proposed OPPs must be computed during the optimization procedure to ensure they respect the available voltage levels. For that reason, the following procedure is adopted:



(a) With $u_0 = 0$

(b) With $u_0 = 1$

(c) With $u_0 = -1$

Fig. 5: Multipolar HWS pulse patterns for $d = 5$.

Step 1: The switching angles α_i and switching transitions Δu_i are derived from the virtual angles γ_i.
Step 2: The computed switching angles α_i are sorted in an ascending order.
Step 3: The switch position u_i is computed by cumulative summing up all the switching transitions starting from the initial switch position until the transition $\Delta u_i(\alpha_i)$, i.e., $u_i = u_0 + \sum_{j=1}^{i} \Delta u_j$, where switching transition Δu_j corresponds to the j^{th} sorted switching angle α_j.

Based on the above analysis, the optimization problem for thermally-constrained multipolar HWS OPPs becomes

$$\begin{aligned}\underset{\boldsymbol{\gamma}_H}{\text{minimize}} \quad & J(\boldsymbol{\gamma}_H) = \textstyle\sum_{n=5,7,11,\ldots} \frac{a_n^2(\boldsymbol{\gamma}_H) + b_n^2(\boldsymbol{\gamma}_H)}{n^2} \\ \text{subject to} \quad & a_1 = 0,\ b_1 = m \\ & 0 \le \gamma_1 < \gamma_2 < \ldots < \gamma_{d-u_0} \le \pi \\ & \pi \le \gamma_{d-u_0+1} < \gamma_{d-u_0+2} < \ldots < \gamma_{2d} \le 2\pi \\ & -1 \le u_i \le 1\ \forall i \in \{1, \ldots, 2d\} \\ & T^{\ell}_{\text{j,max}}(\boldsymbol{\gamma}_H, u_0, \phi) \le T^{\ell}_{\text{j,lmt}}\ \forall \ell \in \{S_{1,2}, D_{1,2,5}\},\end{aligned} \tag{10}$$

where $\boldsymbol{\gamma}_H = [\gamma_1\ \gamma_2\ \ldots\ \gamma_{2d}]^T \in [0, 2\pi]^{2d}$ is the vector of the $2d$ virtual switching angles. Note that, as previously

mentioned, constraint $-1 \leq u_i \leq 1$ is added to (10) to ensure that the derived switching sequences respect the voltage-level limits of a three-level NPC converter. Finally, the junction temperature constraint is a function of not only the virtual angles but also the initial switch position $u_0 \in \{-1, 0, 1\}$.

IV. Numerical Results

This section shows the optimization results for (a) conventional QaHWS OPPs (see problem (1)), (b) thermally-constrained *unipolar* QaHWS OPPs (see problem (1) with constraint (6)), (c) thermally-constrained *unipolar* HWS OPPs (see problem (8)), and (d) thermally-constrained *multipolar* HWS OPPs (see problem (10)). OPPs in the "b" category are hereafter referred to as QaHWS–uni–T_j OPPs, those in category "c" as HWS–uni–T_j OPPs, while those in category "d" as HWS–multi–T_j OPPs. All OPPs are computed for a medium-voltage (MV) drive system consisting of a squirrel cage induction machine with $3.3\,\mathrm{kV}$ rated voltage, $2.8\,\mathrm{kA}$ rated current, $50\,\mathrm{Hz}$ nominal frequency, 0.25 per unit (p.u.) total leakage reactance, and a three-level NPC inverter with a dc-link voltage of $V_\mathrm{dc} = 4.84\,\mathrm{kV}$. The parameters of the considered semiconductor devices are presented in Table I, while the temperature of the cooling water is $T_\mathrm{w} = 37°\mathrm{C}$. For demonstration purposes, OPPs with $d = 5$ and 6 are used, see Figs. 6 and 7 respectively. All OPPs are computed for modulation indices in the range $m \in [0.45, 1.11]$, where the upper limit corresponds to the rated voltage. Note that the modulation index is proportional to the fundamental frequency, while OPPs with higher pulse numbers would be used for $m < 0.65$. Finally, all OPPs are calculated assuming $\phi = 35°$.

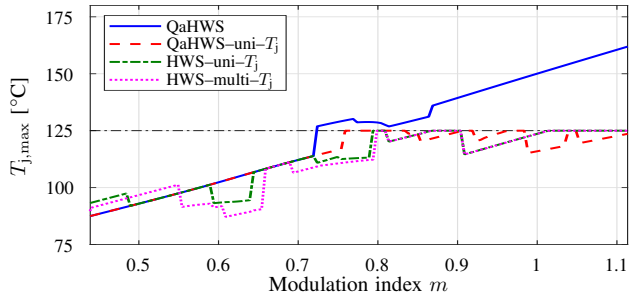
As explained in Section III-B, only the five devices of the upper half of the NPC leg are considered in the optimization problem due to the symmetry of the OPPs. Nevertheless, given the above-mentioned operating conditions, device S_1 is the most thermally stressed device in all considered cases. Since the rest of the devices are well below their thermal limits, only the junction temperate of S_1 is presented hereafter.

Regarding pulse number $d = 5$, the maximum junction temperature $T_{\mathrm{j,max}}$ of device S_1 within the range of considered modulation indices is shown in Fig. 6(a). Therein, the (blue) solid line indicates $T_{\mathrm{j,max}}$ when conventional QaHWS OPPs are used. As can be seen, when the junction temperature is not constrained, the requirement $T_{\mathrm{j,max}} \leq 125°\mathrm{C}$ is violated for a wide range of modulation indices, namely $m \geq 0.72$. Therefore, the switching angles should occur at a lower current to protect the semiconductor device(s).

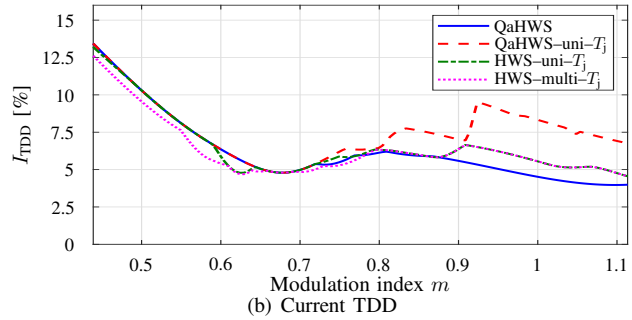
When the junction temperature constraint is implemented, the resulting QaHWS–uni–T_j OPPs respect it for all the aforementioned values of m. This, however, occurs at a cost of an increased current TDD, as can be observed in Fig. 6(b). However, when the symmetry properties are relaxed, HWS–uni–T_j OPPs not only reduce the junction temperature over the whole range of modulation indices but also I_TDD is better than that of QaHWS–uni–T_j OPPs. Regarding this point, when compared with the conventional QHWS OPPs, the maximum relative increase in I_TDD is 85% for QaHWS–uni–T_j OPPs at $m = 1.03$, while it is only 22.1% for HWS–uni–T_j OPPs at the same modulation index. More impressively, when the multipolar patterns are allowed, the junction temperature constraint can be met while the current TDD is even lower than that of QaHWS OPPs. This is thanks to the additional degrees of freedom of problem (10), as it can choose among $2^{d+1} - 1 = 63$ switching sequences and distribute $2d$ angles over a wider range of values. More specifically, multipolar OPPs are selected for $m \in [0.45, 0.66] \cup [0.69, 0.78]$, see Fig. 6(d). Note that in this figure, the unipolar OPP corresponds to pattern $\#47$ (shown with blue solid circles), whereas all other candidate patterns are multipolar OPPs. As can be inferred, using negative switch positions in the first half-period not only relieves the most thermally stressed device but also improves the quality of the output current. For higher modulation indices, multipolar patterns are suboptimal. Still, the relaxation of the symmetry mitigates the expected increase in I_TDD due to the thermal constraint.

Similar observations can be made for $d = 6$, see Fig. 7. The increase in the pulse number, i.e., switching frequency, is expected to result in higher switching losses. Indeed, the maximum junction temperature of device S_1 violates its limit for an even wider range of modulation indices, i.e., $m \geq 0.68$, when conventional QaHWS OPPs are applied. Hence, these OPPs cannot be used in practice in that operating range as they would damage the said device. However, by constraining the junction temperature, the physical requirements can be met for the whole range of examined operating points, but at the expense of deteriorated harmonic performance. Nevertheless, as with $d = 5$, this adverse effect is mitigated when HWS OPPs are applied. Specifically, the implemented symmetry relaxation enables the redistribution of the switching transitions such that the switching events occur at lower currents. Further relaxations in the switching properties result in different distribution of the switching losses among the semiconductor devices of the NPC converter. This is thanks to the fact that, eventually, ten different switching sequences are used over the depicted range of modulation indices. Yet, the proposed OPP problem (10) has the freedom to choose among 127 possible switching sequences when $d = 6$; 126 multipolar and one unipolar (which corresponds to pattern $\#95$ in Fig 7(d)). This highlights the freedom the proposed approach offers to choose among various different patterns that can lead to an improved I_TDD–T_j trade-off.

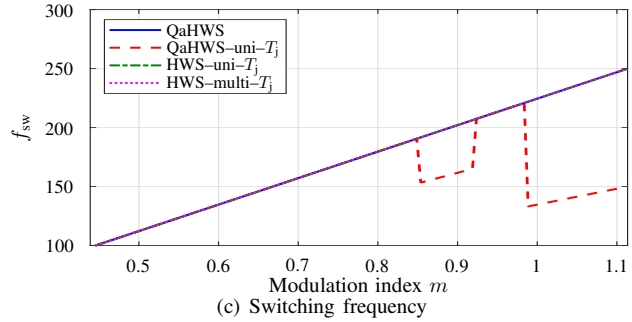
To further highlight the importance of HWS and multipolar OPPs, it is worth discussing the case of QaHWS–uni–T_j OPPs in more detail. Due to the limitations imposed by the symmetry and switching properties, it is not always possible to find a solution with the desired number of switching transitions while still meeting the junction constraint. This behavior becomes more prominent as the modulation index increases, where the search space gets smaller. Since reducing the switching events also reduces the switching losses, OPPs with lower pulse numbers should be used as m increases to meet the thermal constraints. Because of this, the thermally-constrained unipolar QaHWS OPP problem is solved for different values of d, and



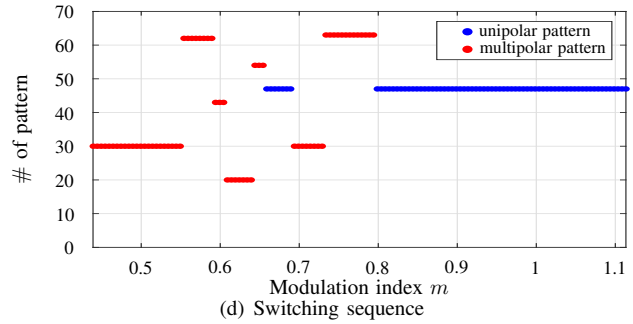
(a) Maximum junction temperature of device S_1



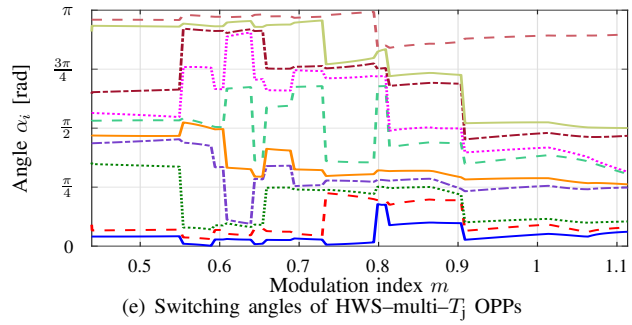
(b) Current TDD



(c) Switching frequency

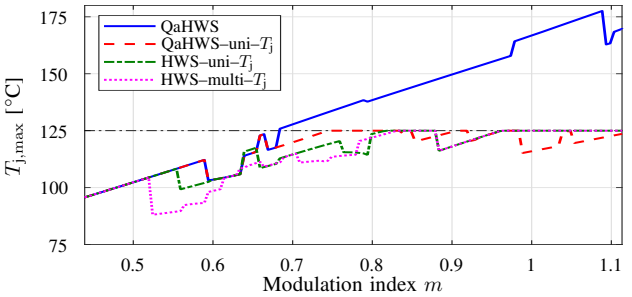


(d) Switching sequence

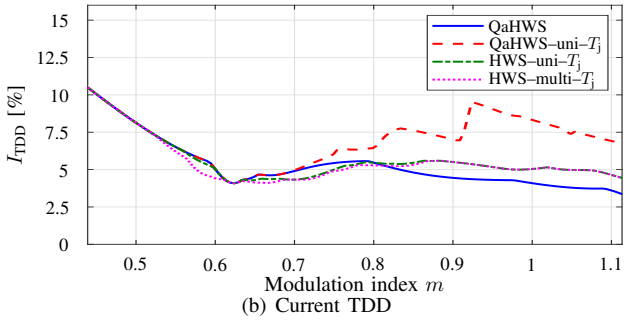


(e) Switching angles of HWS–multi–T_j OPPs

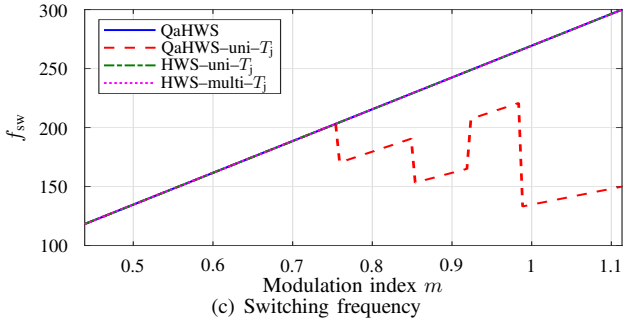
Fig. 6: QaHWS and HWS OPPs for $d = 5$ without and with the T_j constraint. The solid (blue) line corresponds to the conventional QaHWS OPPs, the dashed (red) line to QaHWS–uni–T_j OPPs, the dash-dotted (green) line to HWS–uni–T_j OPPs, and the dotted (pink) line to HWS–multi–T_j OPPs.



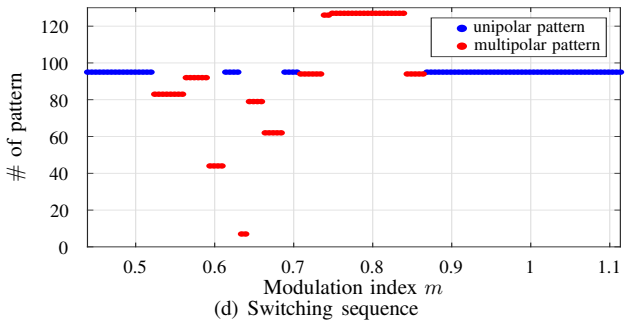
(a) Maximum junction temperature of device S_1



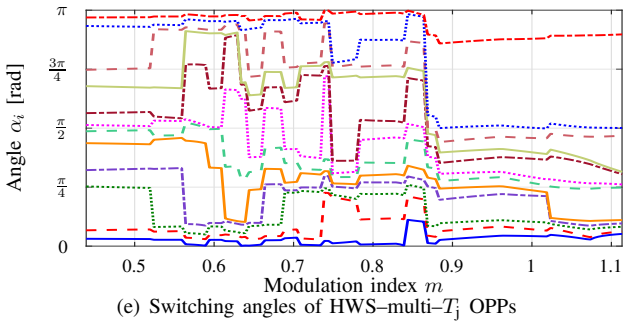
(b) Current TDD



(c) Switching frequency



(d) Switching sequence



(e) Switching angles of HWS–multi–T_j OPPs

Fig. 7: QaHWS and HWS OPPs for $d = 6$ without and with the T_j constraint. The solid (blue) line corresponds to the conventional QaHWS OPPs, the dashed (red) line to QaHWS–uni–T_j OPPs, the dash-dotted (green) line to HWS–uni–T_j OPPs, and the dotted (pink) line to HWS–multi–T_j OPPs.

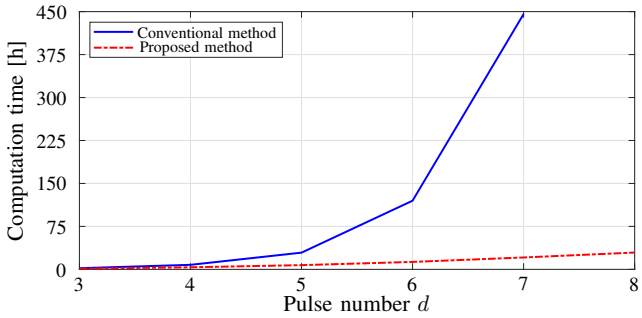


Fig. 8: Computation times of HWS–multi–T_j OPPs with the conventional (blue solid line) and proposed (red dashed-dotted line) methods.

the QaHWS–uni–T_j OPP that results in the lowest I_TDD at a given modulation index is selected in a post-processing step. Taking the $d = 6$ case as an example (see Fig. 7), the selection of lower pulse numbers is visible in Fig. 7(c). Specifically, QaHWS–uni–T_j OPPs with pulse number $d = 6$ are used up to modulation index $m = 0.76$, whereas $d = 5$ is the most suitable pulse number for $m \in [0.76, 0.85] \cup [0.92, 0.98]$. Moreover, four switching transitions are needed in the range $0.85 \leq m \leq 0.92$ to meet the thermal requirements. Finally, QaHWS–uni–T_j OPPs with $d = 3$ are used for $m \geq 0.98$. As QaHWS–uni–T_j OPPs require fewer pulse numbers than the thermally-constrained HWS OPPs (both unipolar and multipolar), the corresponding switching frequency is lower. Consequently, the current quality is compromised, as can also be observed in Fig. 7(b). This clearly demonstrates that the artificial limitations during the computation of thermally-constrained OPPs can result in suboptimal results.

In a last step, the benefits of the proposed OPP problem formulation (10) in terms of computation time are discussed. First, it is worth pointing out, that the conventional solution method would enumerate all 127 possible switching sequences when $d = 6$. In contrast to this, the thermally-constrained multipolar HWS OPP problem needs to be solved only three times with the proposed solution method, enabling a time-efficient computation of the OPPs. To quantify this, Fig. 8 presents the time required by the conventional and proposed solution methods for the computation of HWS–multi–T_j OPPs with different pulse numbers. As can be seen, the conventional solution method requires approximately five days to compute HWS–multi–T_j OPPs with $d = 6$. This is in stark contrast to the time required by the proposed solution, which amounts to only half a day. For pulse number $d = 7$, the savings in computation time are more than 95%, and they are getting bigger with an increasing pulse number.

V. Conclusions

This paper presented the computation of thermally-constrained OPPs. By appropriately imposing a constraint on the junction temperature, the semiconductor devices can be operated at their thermal limits without violating them. Moreover, as demonstrated by the presented numerical results, by relaxing artificial restrictions in the OPPs, such as the OPP symmetry and the polarity of the switch positions, the trade-off between current TDD and junction temperature can be significantly improved. These benefits can be reaped thanks to the proposed OPP problem formulation that brings significant savings in the required computation time, thus facilitating the computation of thermally-constrained multipolar HWS OPPs for several pulse numbers.

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